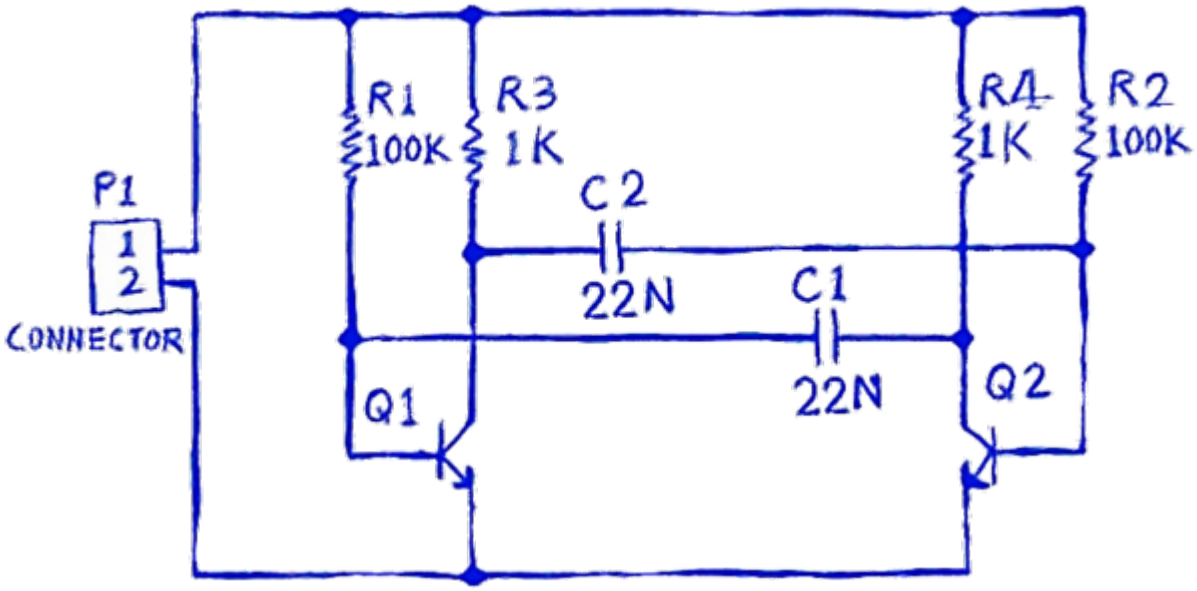
Using Altium Documentation
Modified by Phil Loughhead on Apr 12, 2018

Welcome to the world of electronic product development in Altium's world-class electronic design software. This tutorial will help you get started by taking you through the entire process of designing a simple PCB - from idea to outputs files. If you are new to Altium software then it is worth reading the Exploring Altium Designer page to learn more about the interface, information on how to use panels, and an overview of managing design documents.

To learn more about a command, dialog, object or panel, press **F1** when the cursor is over that item.

The Design

The design you will be capturing and then designing a printed circuit board (PCB) for is a simple astable multivibrator. The circuit is shown below, it uses two general purpose NPN transistors configured as a self-running astable multivibrator.



Circuit for the multivibrator.

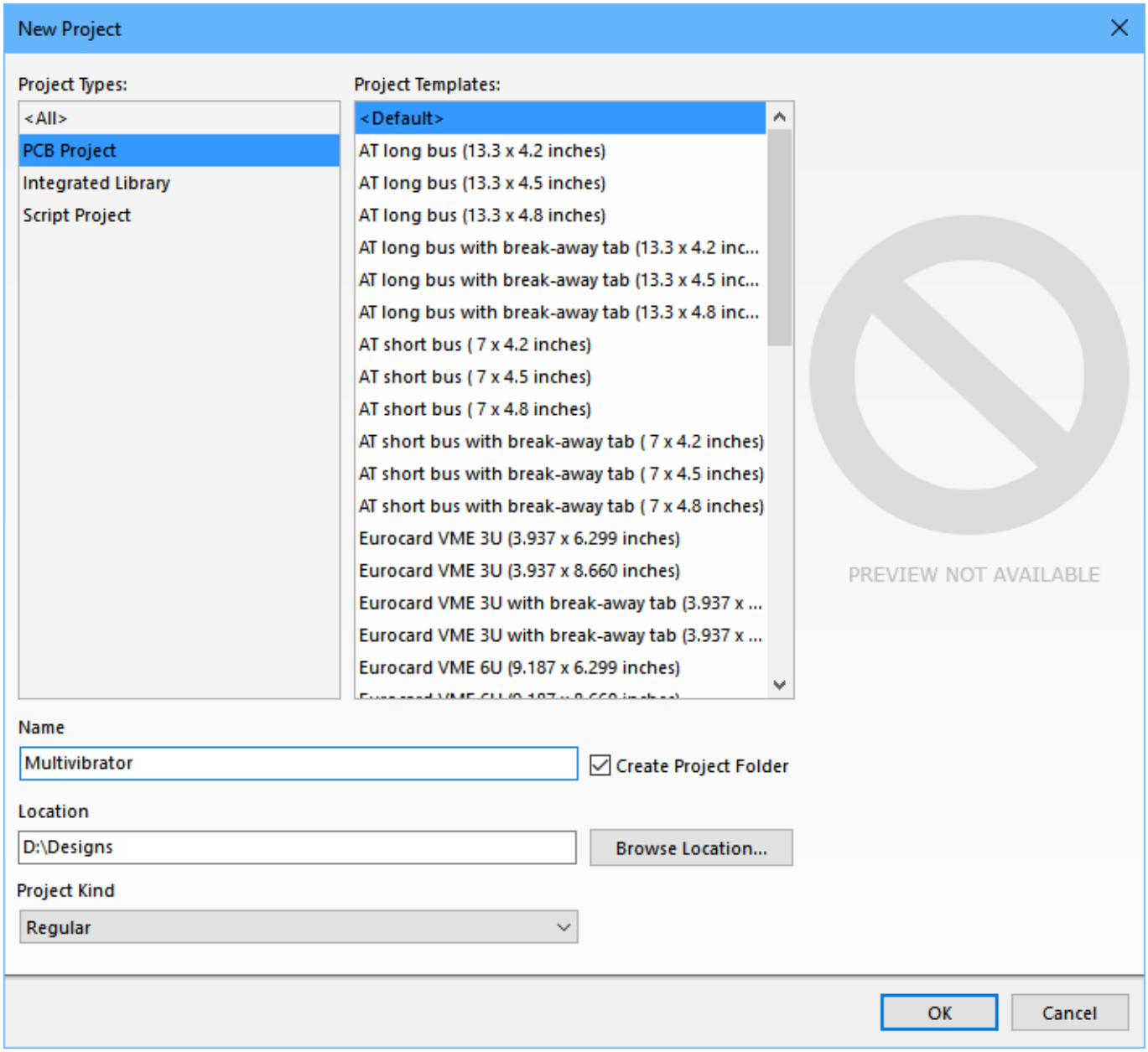
You're ready to begin capturing (drawing) the schematic. The first step is to create a PCB project.

Creating a New PCB Project

Main article: New Project

In Altium's software, a PCB project is the set of design documents (files) required to specify and manufacture a printed circuit board. The project file, for example `Multivibrator.PrjPCB`, is an ASCII file that lists which documents are in the project, as well as other project-level settings, such as the required electrical rule checks, project preferences, and project outputs, such as print and CAM settings.

A new project is created in the *New Project* dialog, as shown below.



Create the new PCB project in the required location.

Creating a new project:

1. Select **File » New » Project** from the menus, the *New Project* dialog will open.
2. Note the list of available **Project Types**, select PCB `Project` if it is not selected.
3. Available templates are listed in the **Project Templates** column, choose `<Default>`.
4. In the **Name** field, enter `Multivibrator`. There is no need to add the file extension, this will be added automatically.
5. Enable the **Create Project Folder** option, this will create a sub-folder below the folder specified in the **Location** field, with the same name as the project.
6. In the **Location** field, type in a suitable location to save the project files, or click **Browse** to

navigate to the required folder.

7. Click **OK** to close the dialog and create the project file in the specified location.
8. The new project will appear in the *Projects* panel. If this panel is not displayed, click the System button at the bottom right of the main design window, and select **Files** from the menu that appears.

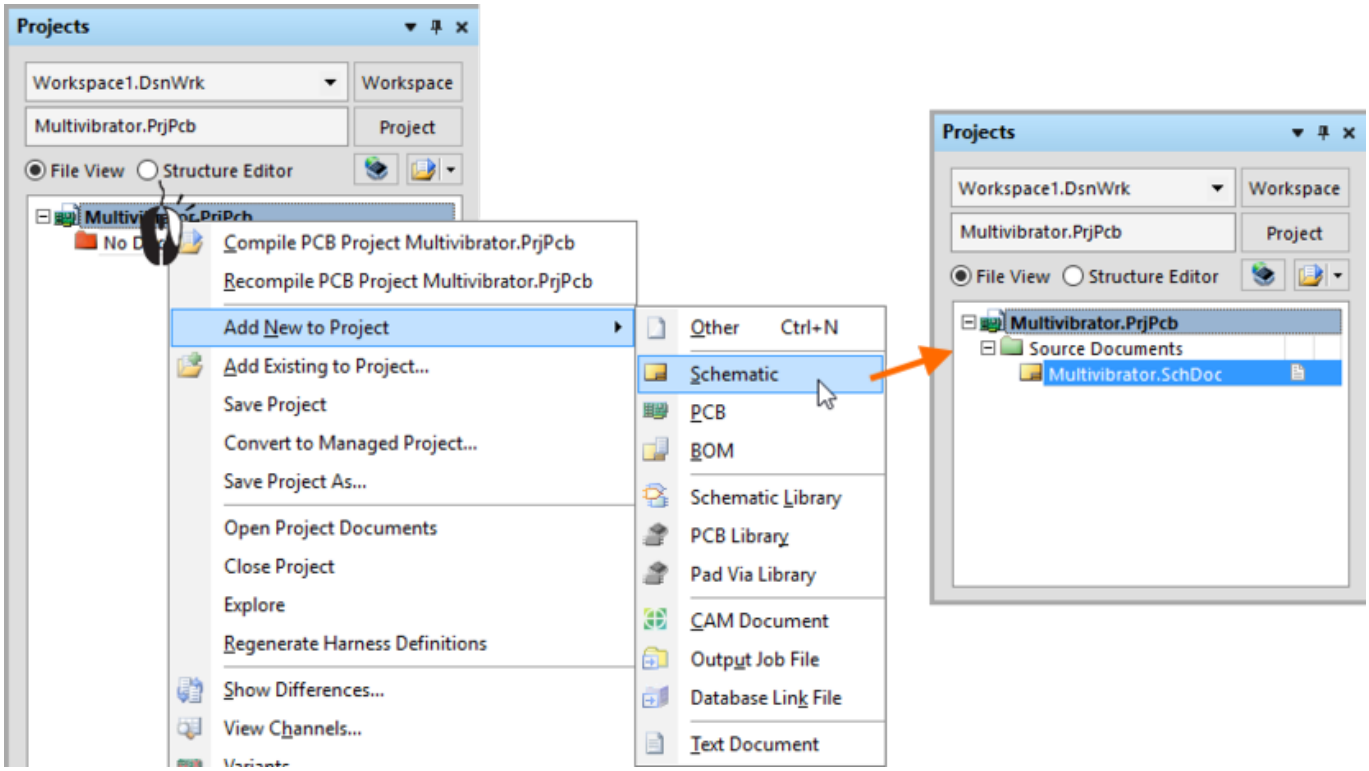
Enabling the **Add Project to Version Control** option will result in the project's source files being stored in an available SVN repository (click **Managed Repositories**), and check out the working copies into the folder specified in the **Location** field. To learn more about version control support, refer to the Version Control and Design Repositories article.

If the **Managed Project** option is enabled, the source files are stored stored in an available SVN repository and the project outputs are stored in an available Altium Vault. To learn more about Managed Projects, refer to the article, The Managed Project and Releasing the Design.

These features will not be used for this tutorial.

Adding a Schematic to the Project

The next step is to add a new schematic sheet to the project.



Add a schematic sheet to the project, name and save the schematic, and save the project.

When the blank schematic sheet opens you will notice that the workspace changes. The main toolbar includes a range of new buttons, new toolbars are visible, the menu bar includes new items, and the *Sheet* panel is displayed - you are now in the Schematic Editor.

The floating panel(s) can be closed using the × icon at the top right of the panel, when needed they can be reopened via the buttons down the bottom right of the application.

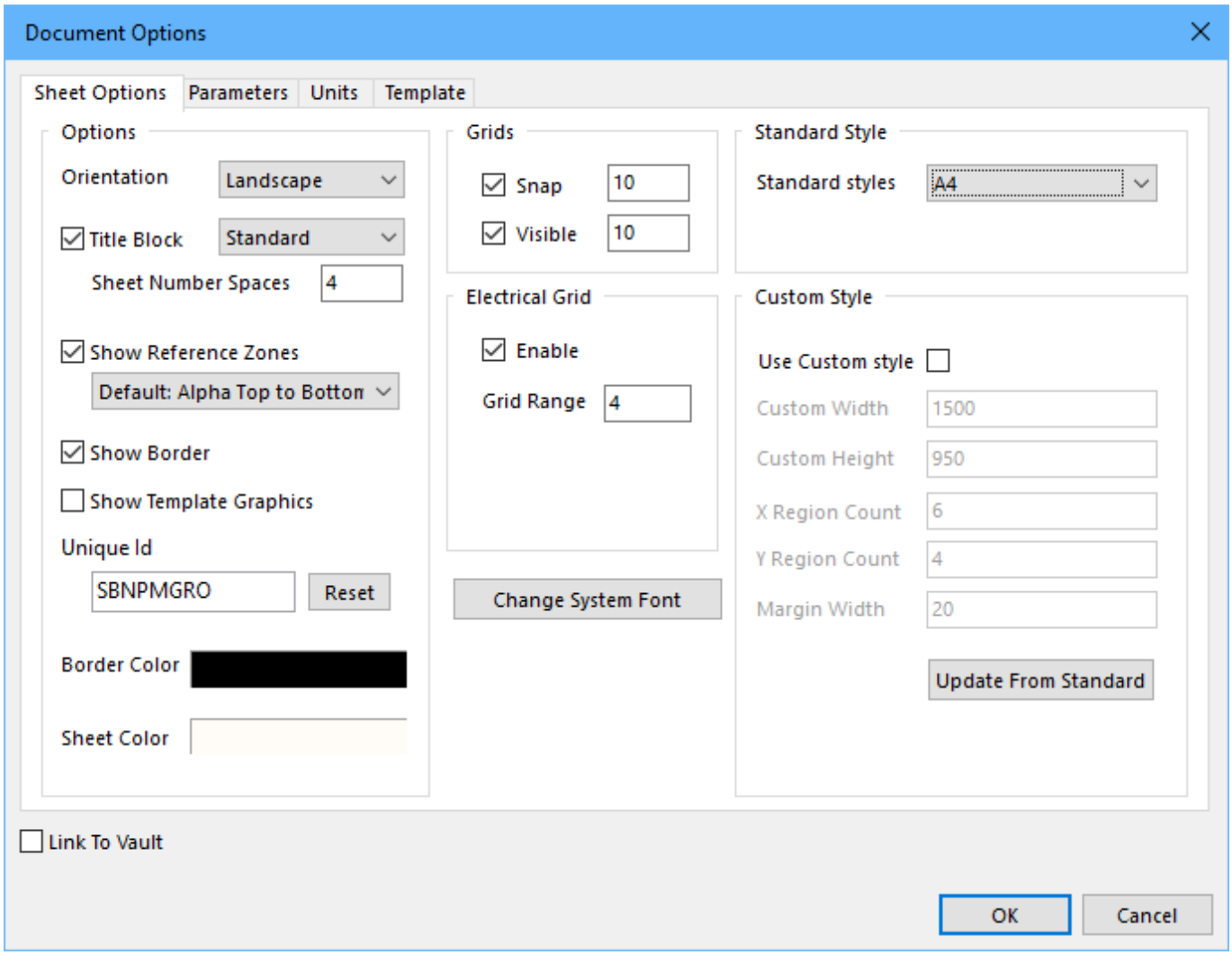
Adding a schematic:

1. **Right-click** on the project filename in the *Projects* panel, and select **Add New to Project » Schematic**. A blank schematic sheet named `Sheet1.SchDoc` will open in the design window and an icon for this schematic will appear linked to the project in the *Projects* panel, under the **Source Documents** folder icon.
2. To save the new schematic sheet, select **File » Save As**. The *Save As* dialog will open, ready to save the schematic in the same location as the project file. Type the name `Multivibrator` in the **File Name** field and click **Save**. Note that files stored in the same folder as the project file itself (or in a child/grandchild folder) are linked to the project using relative referencing, whereas files stored in a different location are linked using absolute referencing.
3. Since you have added a schematic to the project, the project file has changed too. **Right-click** on the project filename in the *Projects* panel, and select **Save Project** to save the project.

Setting the Document Options

Main article: Document Options

Before you start drawing your circuit, is is worth setting up the appropriate document options, including the Sheet Size, and the Snap and Visible grids.



Document options are configured for each schematic sheet, set the sheet size as required.

As well as the technique described in the collapsible section below, the *Document Options* dialog can be opened by double-clicking in the sheet border.

Environment options, such as the cursor type, selection color and auto pan behavior are configured in the *Preferences* dialog (**File » System Preferences**).

Configuring the Document Options:

1. From the menus, choose **Design » Document Options** to open the *Document Options* dialog.
2. For this tutorial, the only change we need to make here is to set the sheet size to A4, this is done in the **Standard Styles** field of the **Sheet Options** tab of the dialog.
3. Confirm that both the **Snap** and **Visible Grids** are set to 10.
4. Click **OK** to close the dialog and update the sheet size.
5. To make the document fill the viewing area, select **View » Fit Document** (shortcut: **V, D**).
6. Save the schematic by selecting **File » Save** (shortcut: **F, S**).

Components and Libraries in Altium Designer

Related article: More about Components and Libraries

This section of the tutorial will explain the two different approaches to working with components (from libraries, or from the Vault). In the following section, you will locate and place the components you need, from the Vault.

The real-world component that gets mounted on the board is represented as a schematic symbol during design capture, and as a PCB footprint for board design. Altium Designer components can be:

- created in and placed from **local libraries**, or
- placed directly from the **Altium Content Vault**, a globally accessible component storage system that contains thousands of components, each with a symbol, footprint, component parameters and links to suppliers.

The following component storage options can be used in Altium Designer:

Library Type	Function
Schematic Library	Schematic component symbols are created in schematic libraries (`*.SchLib`), which are stored locally. Each symbol can become a component by adding links to a PCB footprint, then adding component parameters to detail the component's specifications.
PCB Library	PCB footprints (models) are stored in PCB libraries (`*.PcbLib`), which are stored locally. The footprint includes the electrical elements, such as the pads, as well as the mechanical elements, such as the component overlay, dimensions, glue dots, and so on. It can also include a 3D definition, created by placing 3D Body objects, or by importing a STEP model.
Library Package / Integrated Library	As well as working directly from the schematic and PCB libraries, you can also compile the component elements into an integrated library (`*.IntLib`, stored locally). Doing this results in a single, portable library which holds all the models and symbols. An integrated library is compiled from a Library package (`*.LibPkg`), which is essentially a special-purpose project file, with the source schematic (`*.SchLib`) and PCB libraries (`*.PcbLib`) added to it as source documents. As part of the compilation process, you can also check for potential problems, such as missing models and mismatches between schematic pins and PCB pads.

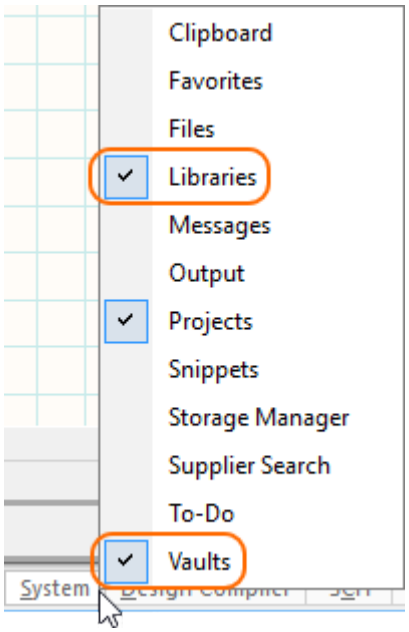
Library Type	Function
Altium Content Vault	The Content Vault is much more than a library. Components are stored in the cloud, accessible from anywhere that has internet access. Content Vault components include: symbol, footprint(s), component parameters, and links to suppliers. They are organized into folders - by manufacturer, or by package type for generics.

Accessing Components

Components are accessed through the:

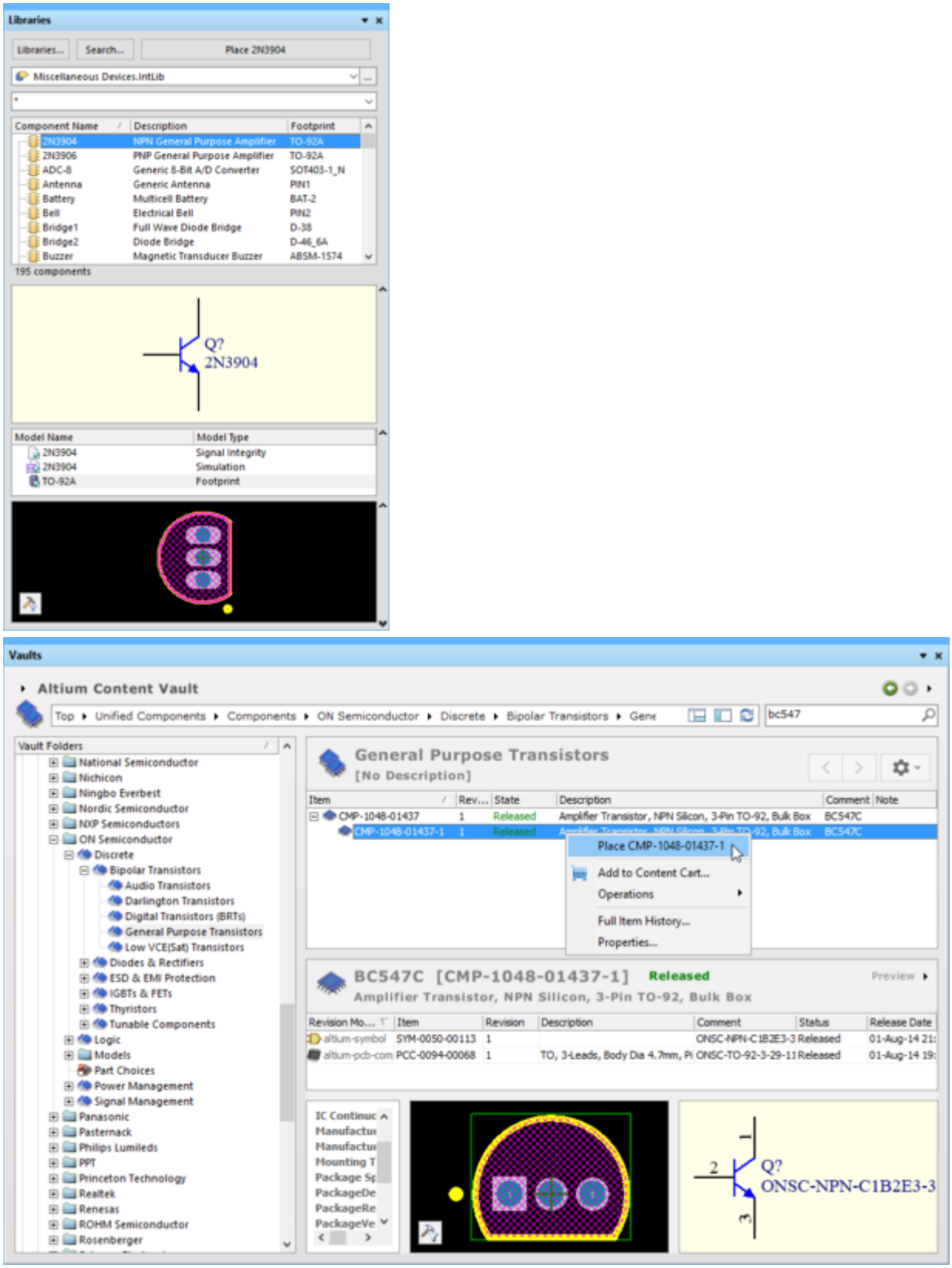
- *Libraries* panel for local library components; or through the
- *Vaults* panel for Content Vault components.

Both of these panels can be accessed via the System menu, click the System button down the bottom right of the application to display the menu.



The menus provides quick access to the panels.

The two panels that are used to access components are shown below.



Access components through either: the *Libraries* panel, or the *Vaults* panel.

Making Libraries Available to Access the Components

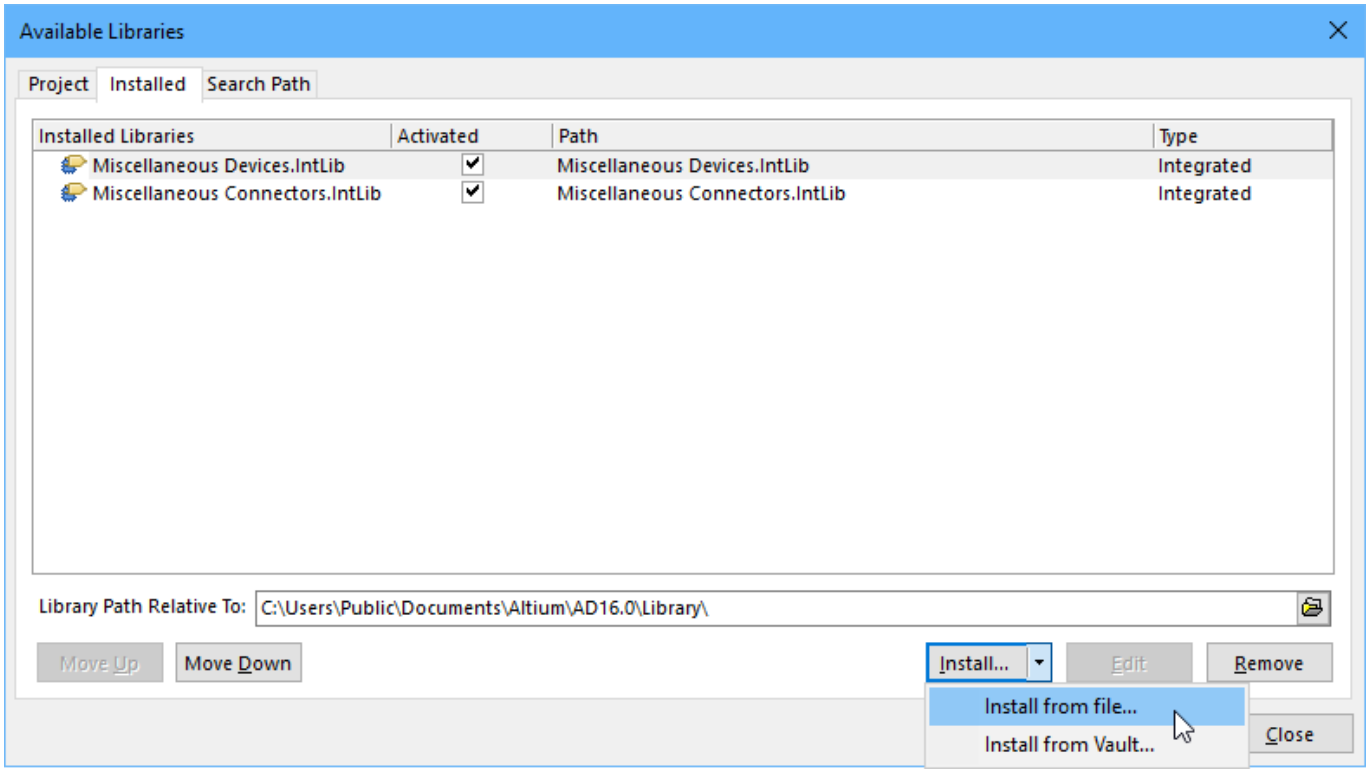
Main article: Available Libraries

In Altium Designer, library-based components can be placed from Available Libraries. The libraries that are available include:

- **Libraries in the current project** - if a library is part of the project, then the components in it

are automatically available for placement within that project.
- **Installed libraries** - these are libraries that have been installed in Altium Designer, their components are available for use in any open project.

Libraries are installed in the **Installed** tab of the *Available Libraries* dialog. To open the dialog, click the **Libraries** button at the top of the *Libraries* panel. If the panel is not currently visible, click **System » Libraries** to display it.



Install the required libraries to make their components available for designs.

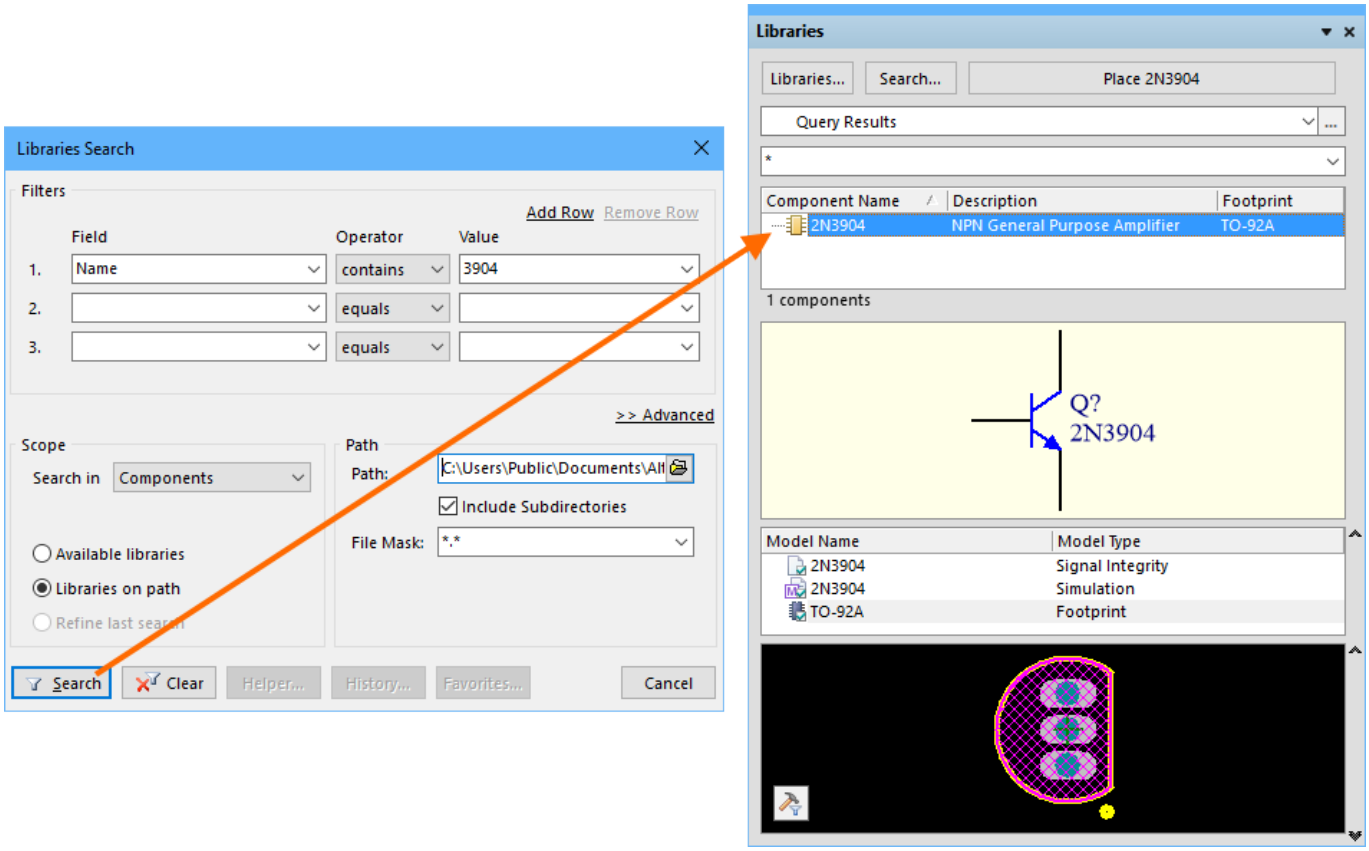
Finding a Component in Libraries

To help you find the component you need, Altium Designer includes powerful library searching capabilities. Although there are components that are suitable for the multivibrator design available in the pre-installed libraries, it is useful to know how to use the search feature to find components.

The *Libraries Search* dialog is accessed by clicking the **Search** button on the *Libraries* panel. The upper half of the dialog is used to define *what* you are searching for, the lower half is used to define *where* to search.

The **Scope** of the search can be in the libraries that are:

- already installed (**Available libraries**), or
- in libraries located in on the hard drive (**Libraries on Path**).

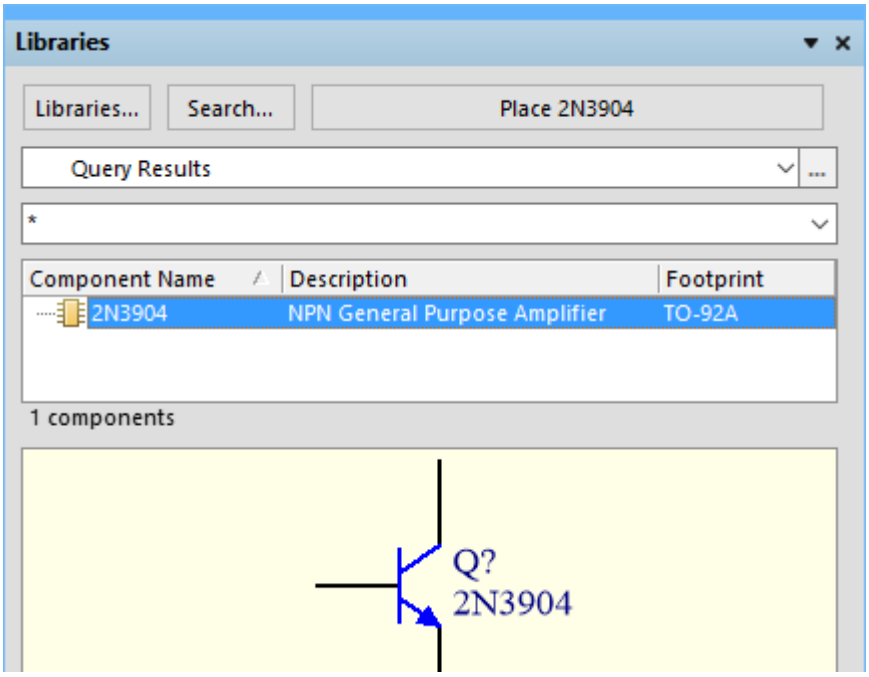


Search for the component using the Libraries Search dialog. You can search across installed libraries (Available libraries), or libraries on the hard drive (Libraries on path).

If you are working from libraries, the first step is to search for a suitable general-purpose NPN transistor, such as a 2N3904. The tutorial components are going to be placed from the Vault, which is discussed shortly.

Searching through libraries:

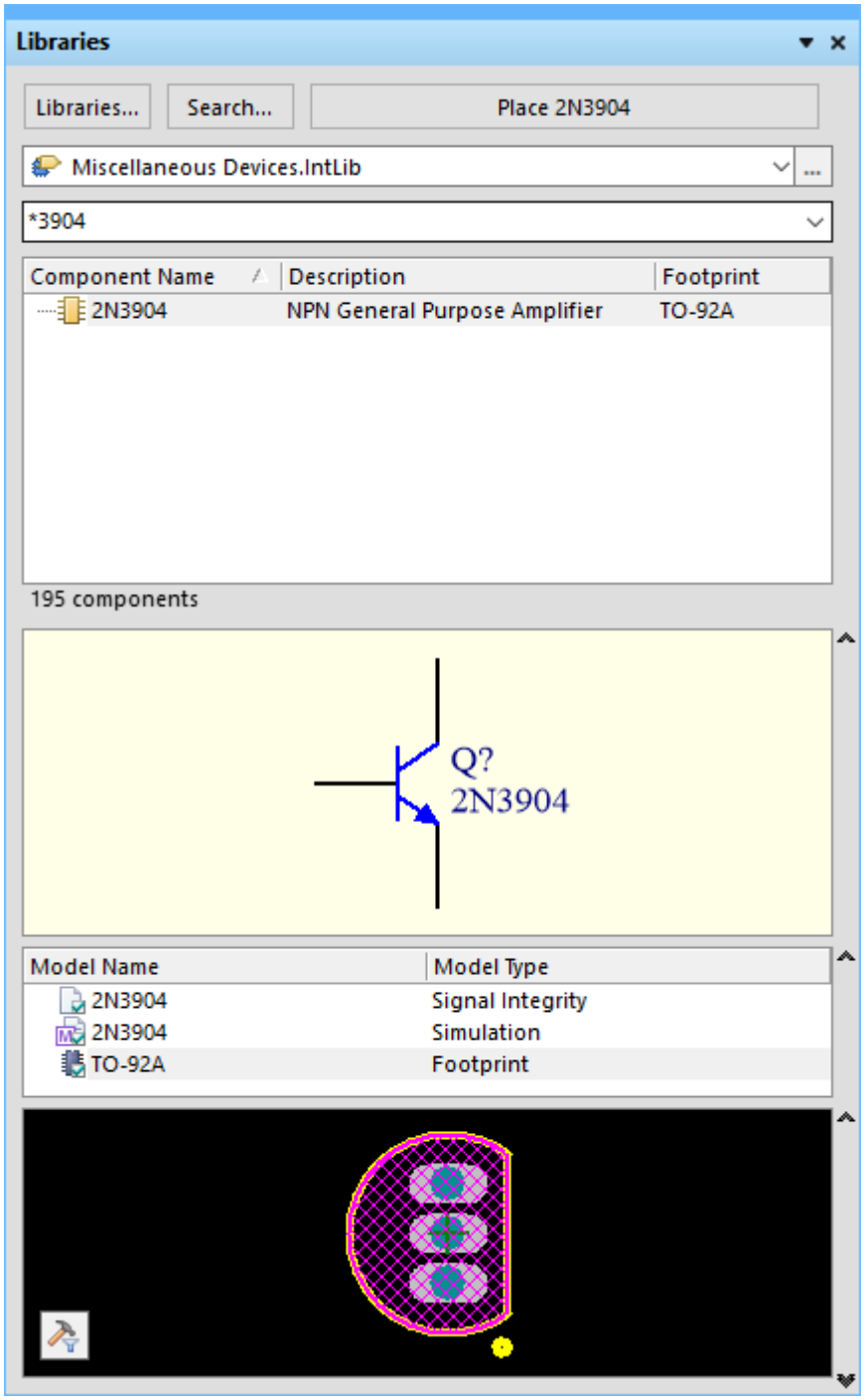
1. If it is not visible, display the *Libraries* panel (**System » Libraries**).
2. Press the **Search** button in the *Libraries* panel to open the *Libraries Search* dialog, as shown above.
3. Ensure that the dialog options are set as follows:
    - For the first **Filter** row, the **Field** is set to `Name`, the **Operator** set to `contains`, and the **Value** is `3904`.
    - The Scope is set to **Search in** `Components`, and **Libraries on path**.
    - The **Path** is set to point to the installed Altium libraries, which will be something like `C:\Users\Public\Documents\Altium\Altium Designer <Version>\Library`.
4. Click the **Search** button to begin the search. The **Query Results** are displayed in the *Libraries* panel as the search takes place - there should be one component found, as shown in the image below.
5. You can only place components from Libraries that are installed in the software, if you attempt to place from a library that is not currently installed you will be asked to **Confirm the installation** of that library when you attempt to place the component.



Library searching is actually performed using queries. In the *Libraries Search* dialog, switch to the **Advanced** mode to examine the query. The query generated by your search configuration should be `(Name LIKE '*3904*')`, if it is not, type this string in and click **Search** again.

Locating a Component in an Available Library

Libraries that are already installed are listed in the drop down at the top of the panel, click to select a library and display the components stored in it. Select the Miscellaneous Devices library from the list, then use the component **Filter** in the panel to locate the required 2N3904 component within the library (as shown in the image below). Since the Miscellaneous Devices library is already installed, this component is ready to place. Do not place it though, instead you will use a transistor from the Altium Content Vault.

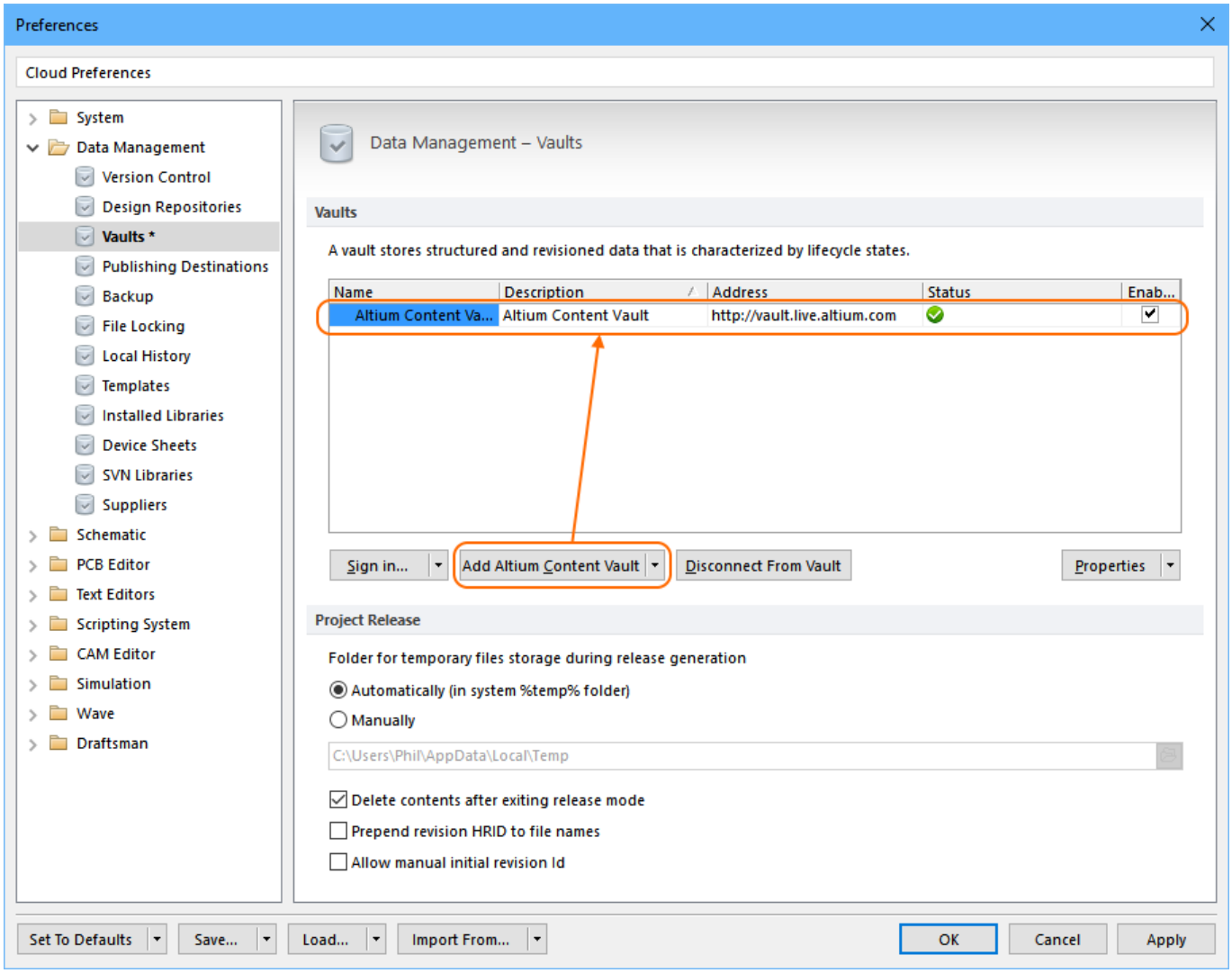


Filtering the library for components with the string 3904 somewhere in their name.

Making the Content Vault Available to Access Components

Main article: Data Management - Vaults

The Altium Content Vault is completely separate from the installed Altium Designer software. To access the components in the Content Vault, you must first connect to it. This is done by clicking the **Add Altium Content Vault** button in the **Data Management - Vaults** page of the *Preferences* dialog.

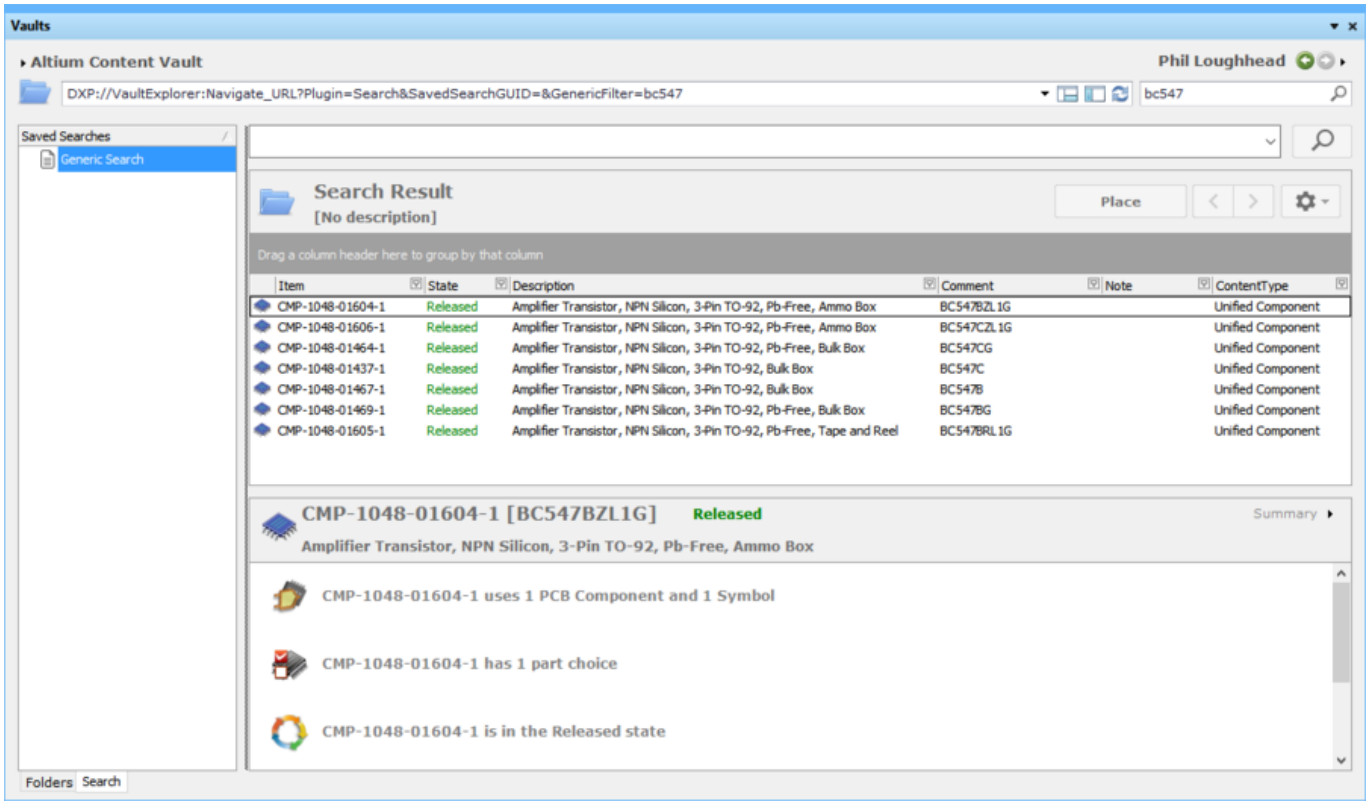


Once you have connected to the Altium Content Vault, you can place components from the Vault into your design.

Finding a Component in the Content Vault

Related article: Vaults panel

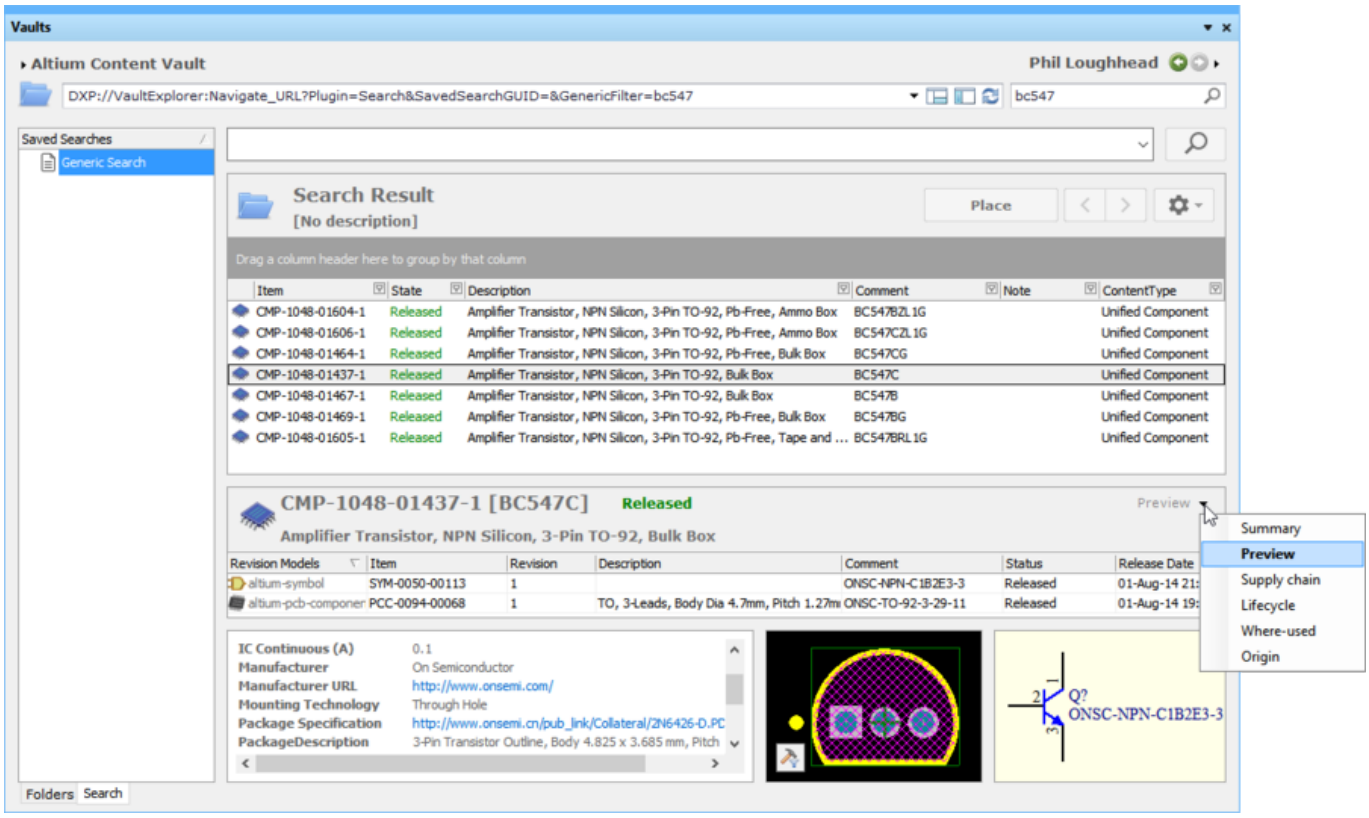
Once you have connected to the Altium Content Vault, you can explore or search for a component. This is done in the *Vaults* panel, select **DXP » Vault Explorer** to display the panel. The panel includes a powerful search feature, enter the search string into the search field at the top-right of the panel, as shown in the image below.



Searching for the general-purpose transistor BC547 in the Altium Content Vault. Click to examine a component of interest.

Working in the Vaults Panel

The Vaults panel includes a number of sections, which can be resized as required. Take some time to explore the features and behavior of the panel, **right-click** for context-specific commands.



Use the Preview mode to examine the models and parameters included with the selected component.

- Components are organized in folders, use the **Vaults Folders** section on the left of the panel to browse through the folders - click the Folders tab down the bottom to display them.

- There is a large number of components stored in the Altium Content Vault, it can be more efficient to search, as just described.
- The lower region of the panel has a number of display modes, including: **Summary**, **Supply Chain**, **Where-used**, and **Preview**. Use the down-arrow icon to select the required mode, as shown in the image above.
- To see which folder a found component is stored in, right-click on the component and select the **Navigate To** command.
- Use the  button at the top-right of the panel to return to the search results.

Placing Components on the Schematic

Components are placed from the *Libraries* or *Vaults* panel onto the current schematic sheet. This can be done by:

From the Libraries Panel

Main article: Libraries Panel

- **Clicking the Place button** - the component appears floating on the cursor, position it and click to place.
- **Double-clicking** - double-click the component in the list of components in the panel, the component appears floating on the cursor, position it and click to place.
- **Click and drag** - click and drag the component onto this sheet, this mode requires that the cursor is held down, the component is placed when the cursor is released.

From the Vaults Panel

Main article: Vaults Panel

- **Right-click** on the component and select **Place**, the component appears floating on the cursor, position it and click to place. Note that if the *Vaults* panel is floating over the workspace, it will fade to allow you to see the schematic and place the component.
- **Click and drag** - click and drag the component from the *Vaults* panel and drop it onto the schematic. This mode requires that the cursor is held down, the component is placed when the cursor is released. Depending on the speed of your internet connection, there may be a brief delay before the component is placed.

Placement Tips

While the component is floating on the cursor, you can:

- Press **Spacebar** to rotate it anti-clockwise, in 90 degree increments.
- Press **X** to flip it along the X-axis, press **Y** to flip it along the Y-axis.
- Press **Tab** to edit the properties of an object prior to placement, the values entered become the defaults, and the designator is auto-incremented.
- During component placement the software will automatically pan if you touch the window edge. If you accidentally pan beyond where you want, while the component is floating on the cursor you can:
  - **Ctrl+Wheel Roll** too zoom out and in again, or
  - **right-click and drag** to slide the schematic around, or
  - **Ctrl+PgDn** to display the entire sheet again.

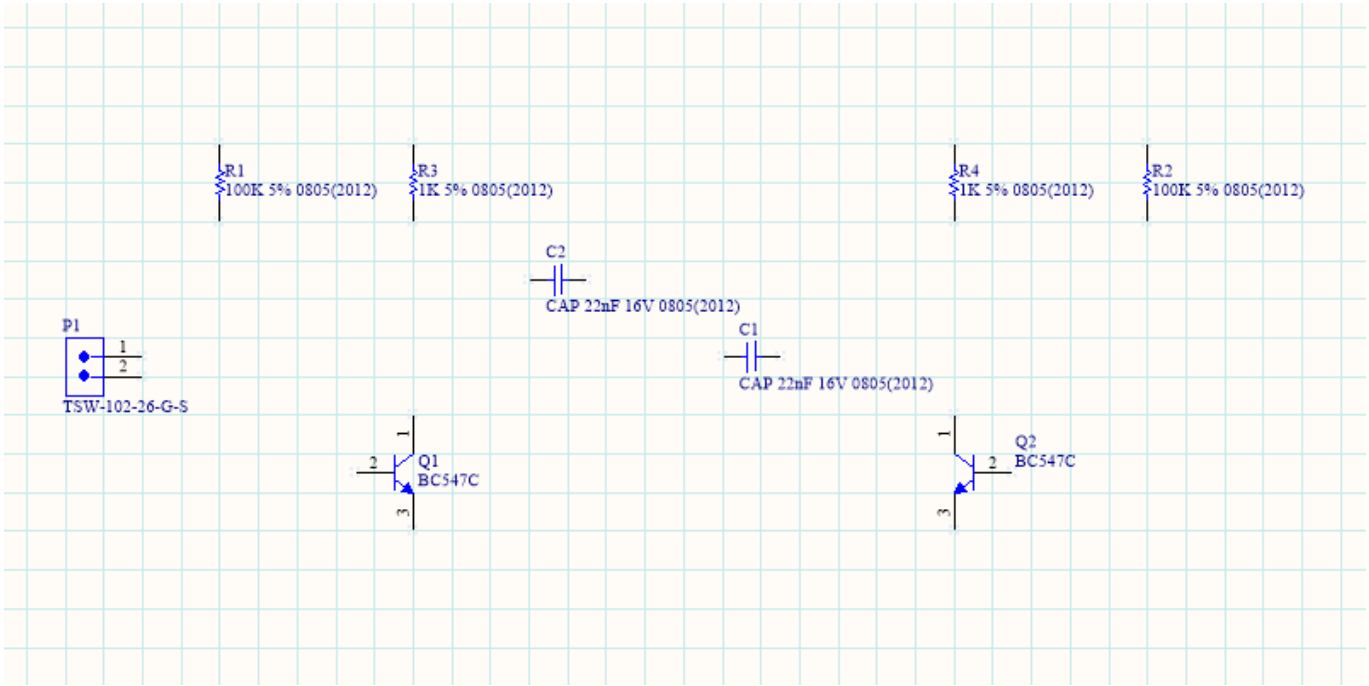
Multivibrator Parts

The next step is to search the Content Vault for the following componentsto use in the Multivibrator circuit.

Designator	Description	Vault Item-Revision or Library Component Name	Comments
Q1, Q2	General purpose NPN transistor, eg BC547 or 2N3904	CMP-1048-01437-1	searched Vault for BC547, chose the first one
R1, R2	100K resistor, 5%, 0805	CMP-1013-00122-1	searched Vault for `100K 5% 0805`
R3, R4	1K resistor, 5%, 0805	CMP-1013-00074-1	searched Vault for `1K 5% 0805`, note that search also returns 1K3, 1K8, etc
C1, C2	22nF capacitor, 10%, 16V, 0805	CMP-1036-04042-1	searched Vault for `22nF 16V 0805`
P1	2-pin header, thruhole	CMP-1024-00327-1	searched Vault for `header, 2-pin, vertical`

Once you have placed the components, the schematic should look like the image below.

You can proceed to find and place the components. Note that the collapsible sections below include tips on editing during placement, which is more efficient. If you choose to leave the editing until after the components are placed, double-click on a component to edit it.



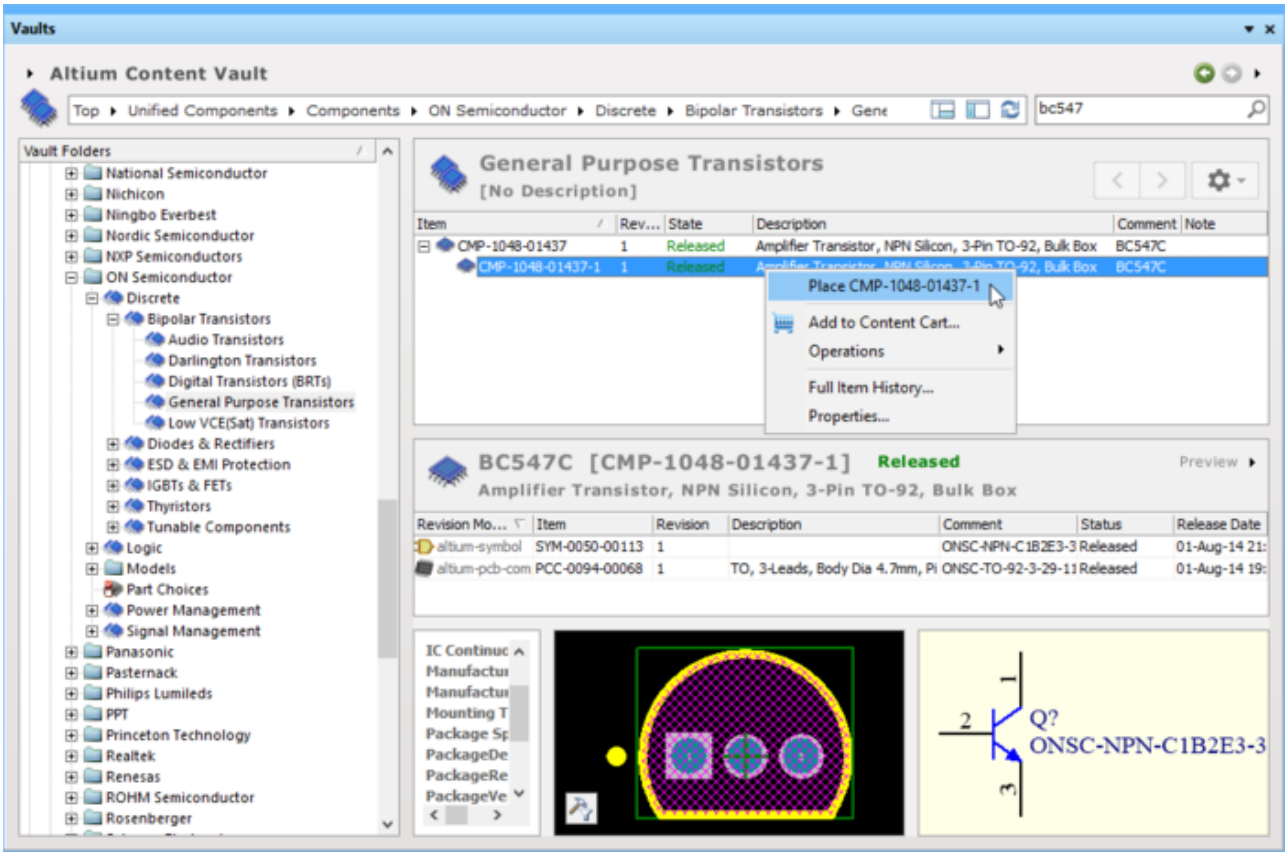
All the components have been placed, ready for wiring.

[Finding and Placing the Transistors:]

1. Select **View » Fit Document** (shortcut: **V, D**) to ensure your schematic sheet takes up the full

window.

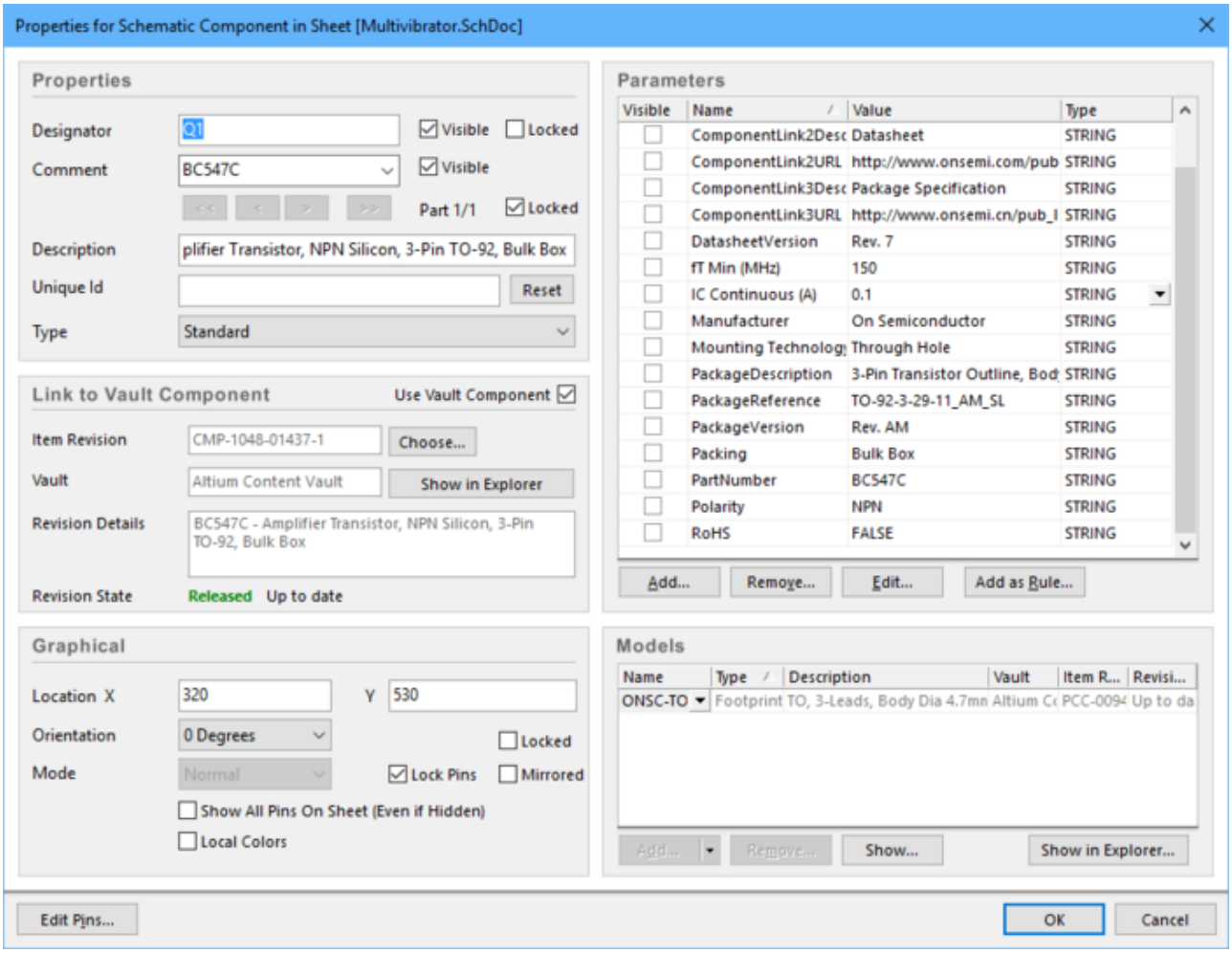
2. Using the search techniques just described, use the *Vault* panel to search and locate the transistor, BC547.
3. When you search the Vault, it will first cluster the results to show the folders that contains possible components. For the transistor search, all results are in the same folder, named `General Purpose Transistors`. Click the hyperlink to open the search results for that folder, then click the first Item, `CMP-1048-01437-1`.
4. That component will be presented in the *Vaults* panel, where you can display the **Preview** down the bottom and examine the symbol, footprint and component parameters (you might need to resize the lower section to display all of the Preview content).



5. **Right-click** on the transistor's Item-Revision number to display the context menu (as shown above), then select **Place CMP-1048-01437-1** from the menu. The cursor will change to a cross hair and you will have an image of the transistor *floating* on your cursor. You are now in part placement mode. If you move the cursor around, the transistor will move with it.

   Do not place the transistor yet!

6. Before placing the part on the schematic you can edit its properties - which can be done for any object floating on the cursor. While the transistor is still floating on the cursor, press the **Tab** key to open the *Component Properties* dialog. You can now set up the dialog options to appear as below.



Set the Designator to Q1, and the Comment to be Visible.

7. In the **Properties** section of the dialog, type in the **Designator** Q1.
8. Confirm that the **Visible** checkbox for the **Comment** field is enabled.
9. Leave all other fields at their default values, and click **OK** to close the dialog.
10. Move the cursor, with the transistor symbol attached, to position the transistor a little to the left of the middle of the sheet. Note the current snap grid, it is displayed on the left of the Status bar down the bottom of the application. It defaults to 10, you can press the G shortcut to cycle through the available grid settings during object placement. It is strongly advised to keep the snap grid at 10 or 5, to keep the circuit neat, and make it easy to attach wires to pins. For a simple design such as this, 10 is a good choice.
11. Once you are happy with the transistor's position, left mouse click or press **Enter** on the keyboard to place the transistor onto the schematic.
12. Move the cursor and you will find that a copy of the transistor has been placed on the schematic sheet, but you are still in part placement mode with the part outline floating on the cursor. This feature allows you to place multiple parts of the same type.
13. You are ready to place the second transistor. This transistor is the same as the previous one, so there is no need to edit its attributes before you place it. The software will automatically increment the component designator when you place multiple instances of the same part. In this case, the next transistor will automatically be designated Q2.
14. If you refer to the schematic diagram shown before, you will notice that Q2 is drawn as a mirror of Q1. To horizontally flip the orientation of the transistor floating on the cursor, press the **X** key on the keyboard. This flips the component along the X axis.
15. Move the cursor to position the part to the right of Q1. To position the component more accurately, press the **PgUp** key twice to zoom in two steps. You should now be able to see the grid lines.

16. Once you have positioned the part, left mouse click or press **Enter** to place Q2. Once again a copy of the transistor you are "holding" will be placed on the schematic, and the next transistor will be floating on the cursor ready to be placed.
17. Since all the transistors have been placed, exit part placement mode by clicking the **Right Mouse Button** or pressing the **ESC** key. The cursor will revert back to a standard arrow.

Finding and Placing the Resistors:

1. Using the search techniques just described, search for a suitable `100K 5% 0805` resistor in the *Vaults* panel. The search should return the Item-Revision CMP-1013-00122-1.
2. **Right-click** on the resistor's Item-Revision number to display the context menu, then select **Place CMP-1013-00122-1** from the menu.
3. While the resistor is still floating on the cursor, press the **Tab** key to open the *Component Properties* dialog.
4. In the **Properties** section of the dialog, type in the **Designator** R1.
5. Confirm that the **Visible** checkbox for the **Comment** field is enabled.
6. Ensure that the footprint Model is set to RESC0805(2012)_N. Using the dropdown next to the Model name you will see that there are 3 footprint models attached to this component, IPC Low Density (_M), IPC Medium Density (_N) & IPC High Density (_L). The footprint selected here will be transferred to the PCB during design synchronization.
7. Leave all other fields at their default values and click **OK** to close the dialog, the resistor will be floating on the cursor.
8. Press the **Spacebar** to rotate the component in 90° increments, until it has the correct orientation.
9. Position the resistor above and to the left of the base of Q1 (refer to the schematic diagram shown earlier) and click the **Left Mouse Button** or press **Enter** to place the part.
10. Next place the other 100k resistor, R2, above and to the right of the base of Q2. The designator will automatically increment when you place the second resistor.
11. Exit part placement mode by clicking the **Right Mouse Button** or pressing the **ESC** key. The cursor will revert back to a standard arrow.
12. The remaining two resistors, R3 and R4, have a value of 1K, search for a suitable `1K 5% 0805` resistor in the *Vaults* panel.
13. This search will return all resistors whose values start with 1K, including 1K1, 1K2, 1K3, and so on. Using the **Description** column in the *Vaults* panel to help locate the 1K resistor, click in the search results to open the `1K 5% 0805` resistor, then **right-click** and **Place CMP-1013-00074-1**.
14. Using the steps just given, set the **Designator** to R3, confirm that the **Comment** field is displayed, and set the footprint Model to RESC0805(2012)_N.
15. Position and place R3 directly above the Collector of Q1, then place R4 directly above the Collector or Q2, as shown in the image above.
16. **Right-click** or press **ESC** to exit part placement mode.

Finding and Placing the Capacitors:

1. Return to the *Vaults* panel, and search for a suitable `22nF 16V 0805` capacitor. The search will return a number of potential capacitors, click on Item `CMP-1036-04042-1` to use in this design.
2. **Right-click** on the capacitor's Item-Revision number and select **Place CMP-1036-04042-1** from the menu.
3. While the capacitor is still floating on the cursor, press the **Tab** key to open the *Component Properties* dialog.
4. In the **Properties** section of the dialog, type in the **Designator** C1.

5. Confirm that the **Visible** checkbox for the **Comment** field is enabled.
6. Ensure that the footprint Model is set to `CAPC0805(2012)145_N`.
7. Leave all other fields at their default values and click **OK** to close the dialog, the capacitor will be floating on the cursor.
8. Press the **Spacebar** to rotate the component in 90° increments, until it has the correct orientation.
9. Position the capacitor above the transistors but below the resistors (refer to the schematic diagram shown earlier) and click the **Left Mouse Button** or press **Enter** to place the part.
10. Position and place capacitor C2.
11. **Right-click** or press **Esc** to exit placement mode.

Finding and Placing the Connector:

1. Return to the *Vaults* panel, and search for `header, 2-pin, vertical` to locate a suitable connector. The search will return a number of potential terminal strips, some with 0.1" pitch, some with 2mm pitch, as shown by the text in the **Path** column.
2. Using the **Path** information to help, click on the Terminal Strips results that are in the `\.100-inch Square Post` Vault folder.
3. The search results list will change to show the 9 suitable headers that are in that folder. From the **Description** column you will see that some are low profile, one is a press fit, and four are standard through-hole headers.
4. From those that are standard through-hole headers, select `CMP-1024-00327-1` from the list to jump to that Vault component.
5. **Right-click** on the header's Item-Revision number and select **Place CMP-1024-00327-1** from the menu.
6. While the header is floating on the cursor, press **Tab** to edit the attributes and set **Designator** to P1.
7. Before placing the header, press **Spacebar** to rotate it to the correct orientation. Click to place the connector on the schematic, as shown in the image above.
8. **Right-click** or press **ESC** to exit part placement mode.
9. Save your schematic (shortcut: **F, S**).

You have now placed all the components. Note that the components shown in the image above are spaced so that there is plenty of room to wire to each component pin. This is important because you can not place a wire across the bottom of a pin to get to a pin beyond it. If you do, both pins will connect to the wire. If you need to move a component, click-and-hold on the body of the component, then drag the mouse to reposition it.

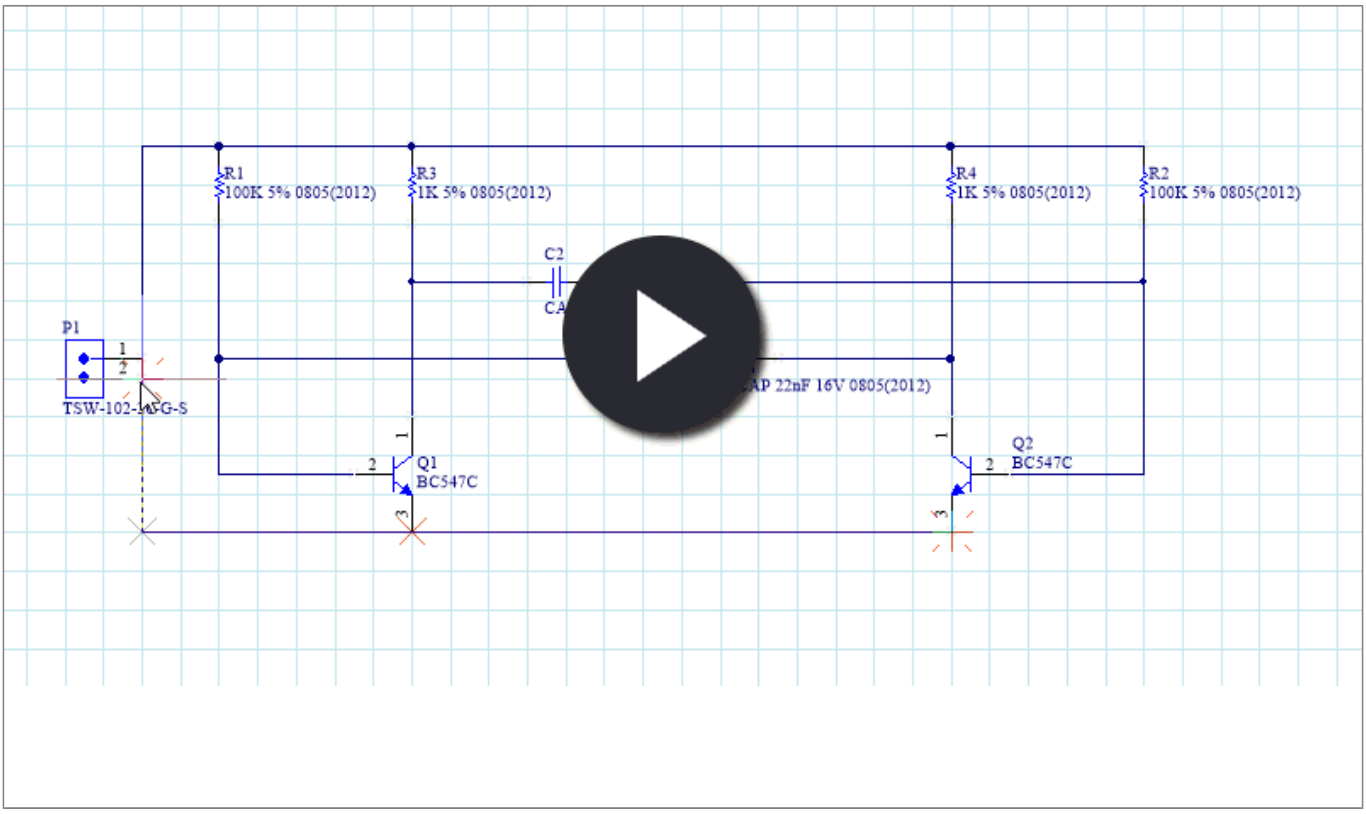
Component Positioning Tips

- To reposition any object, place the cursor directly over the object, click-and-hold the left mouse button, drag the object to a new position and then release the mouse button. Movement is constrained to the current snap grid, which is displayed on the Status bar, press the **G** shortcut at any time to cycle through the current snap grid settings. Remember that it is important to position components on a coarse grid, such as 5 or 10.
- You can also re-position a group of selected schematic objects using the arrow keys on the keyboard. Select the objects, then press an **arrow key** while holding down the **Ctrl** key. Hold **Shift** as well to move objects by 10 times the current snap grid.
- The grid can also be temporarily set to 1 while moving an object with the mouse, hold **Ctrl** to do this. Use this feature when positioning text.

- The grids you cycle through when you press the **G** shortcut are defined in the **Schematic - Grids** page of the *Preferences* dialog (**File » System Preferences**). On the **Schematic - General** page of the *Preferences* dialog there are settings to select the type of units that will be used, select between **Imperial** or **Metric**. Note that Altium components are designed using the **DXP Defaults** imperial grid, if you change to a metric grid the component pins will no longer fall onto a grid of 10 - because of this, it is recommended to use the DXP Defaults grid unless you plan on only using your own components.

Wiring up the Circuit

Wiring is the process of creating connectivity between the various components of your circuit. To wire up your schematic, refer to the sketch of the circuit and the animation shown below.



Use the Wiring tool to wire up your circuit, towards the end of the animation you can see how wires can be dragged.

Wiring the schematic:

1. To make sure you have a good view of the schematic sheet, press the **PgUp** key to zoom in or **PgDn** to zoom out. Alternatively, hold down the **Ctrl** key and roll the mouse wheel to zoom in/out, or hold **Ctrl + Right Mouse** button down and drag the mouse up/down to zoom in/out. There are also a number of useful View commands in the right-click **View** submenu, such as **Fit All Objects** (**Ctrl+PgDn**).
2. Firstly, wire the lower pin of resistor R1 to the base of transistor Q1 in the following manner. Click the button (**Place » Wire**) to enter the wire placement mode. The cursor will change to a cross hair.
3. Position the cursor over the bottom end of R1. When you are in the right position, a red connection marker (large cross) will appear at the cursor location. This indicates that the cursor is over a valid electrical connection point on the component.
4. Click the **Left Mouse Button** or press **Enter** to anchor the first wire point. Move the cursor and

you will see a wire extend from the cursor position back to the anchor point.

5. Position the cursor over the base of Q1 until you see the cursor change to a red connection marker. If the wire is forming a corner in the wrong direction, press **Spacebar** to toggle the corner direction.
6. Click or press **Enter** to connect the wire to the base of Q1. The cursor will release from that wire.
7. Note that the cursor remains a cross hair, indicating that you are ready to place another wire. To exit placement mode completely and go back to the arrow cursor, you would **Right-Click** or press **ESC** again - but don't do this just now.
8. Next wire from the lower pin of R3 to the collector of Q1. Position the cursor over the lower pin of R3 and click or press **Enter** to start a new wire. Move the cursor vertically till it is over the collector of Q1, and click or press **Enter** to place the wire segment. Again the cursor will release from that wire, and you remain in wiring mode, ready to place another wire.
9. Wire up the rest of your circuit, as shown in the animation above.
10. When you have finished placing all the wires, **right-click** or press **ESC** to exit placement mode. The cursor will revert to an arrow.

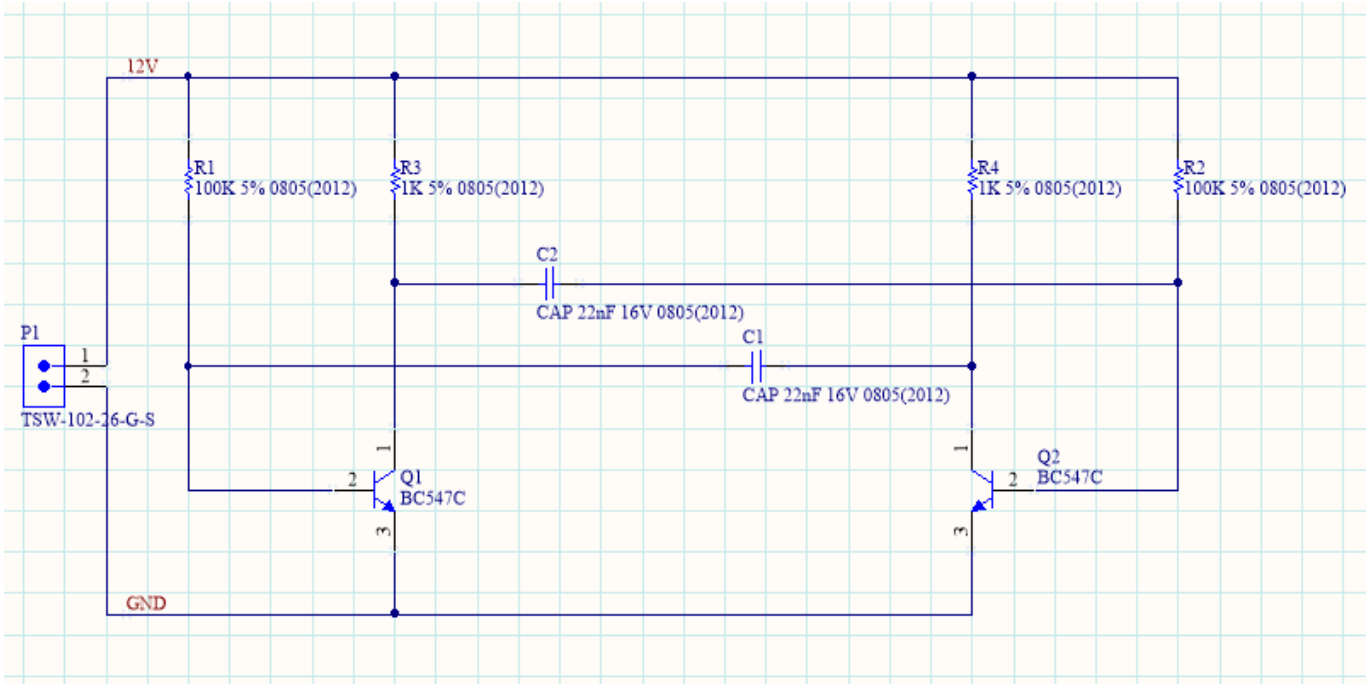
Wiring Tips

- Left-click or press **Enter** to anchor the wire at the cursor position.
- Press **Backspace** to remove the last anchor point.
- Press **Spacebar** to toggle the direction of the corner. You can observe this in the animation shown above, when the connector is being wired.
- Press **Shift+Spacebar** to cycle through the wiring corner modes. Available modes include: 90, 45, Any Angle and Autowire (place orthogonal wire segments between the click points).
- **Right-click** or press **Esc** to exit wire placement mode.
- **Click and hold** to move a placed component, or **Ctrl + click and hold** to drag the component together with any connected wires.
- **Ctrl+click and hold** on a wire to drag the wire, as shown in the animation above.
- Whenever a wire crosses the connection point of a component, or is terminated on another wire, a junction will automatically be created.
- A wire that crosses the end of a pin will connect to that pin, even if you delete the junction. Check that your wired circuit looks like the figure shown, before proceeding.
- Wiring cross-overs can be displayed as a small arch if preferred, enable the option in the **Schematic - General** page of the *Preferences* dialog.

Nets and Net Labels

Each set of component pins that you have connected to each other now form what is referred to as a *net*. For example, one net includes the base of Q1, one pin of R1 and one pin of C1. Each net is automatically assigned a system-generated name, which is based on one of the component pins in that net.

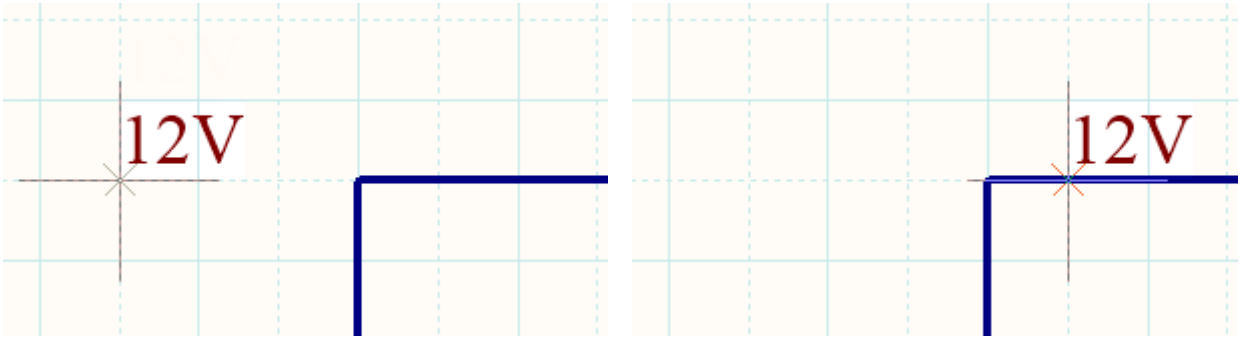
To make it easy to identify important nets in the design, you can add Net Labels to assign names. For the multivibrator circuit, you will label the 12V and GND nets in the circuit, as shown below.



Net Labels have been added to the 12V and GND nets, completing the schematic.

[Adding net labels:]

1. Click the Net button (**Place » Net Label**). A net label will appear floating on the cursor.
2. To edit the net label before it is placed, press **Tab** key to open the *Net Label* dialog.
3. Type 12V in the **Net** field, then click **OK** to close the dialog.
4. Place the net label so that the bottom left corner of the net label touches the upper most wire on the schematic, as shown in the image below. The cursor will change to a red cross when the net label is correctly positioned to connect to the wire. If the cross is light grey, it means there will not be a valid connection made.



The net label in free space (left image) and positioned over a wire (right image), note the red cross.

5. After placing the first net label you will still be in net label placement mode, so press the **Tab** key again to edit the second net label before placing it.

6. Type GND in the **Net** field and click **OK** to close the dialog.
7. Place the net label so that the bottom left of the net label touches the lower most wire on the schematic (as shown in the image below). **Right-click** or press **ESC** to exit net label placement mode.
8. Save your circuit, and the project as well.

Net Labels, Port and Power Ports

- As well as giving a net a name, Net Labels are also used to create connectivity between 2 separate points on the *same* schematic sheet.
- Ports are used to create connectivity between 2 separate points on *different* sheets. Offsheet connectors can also be used to do this.
- Power Ports are used to create connectivity between points on all sheets, for this design Net Labels or Power Ports could have been used.

Congratulations! You have just completed your first schematic capture. Before you turn the schematic into a circuit board you need to configure the project options, and check the design for errors.

Setting Up Project Options

Project-specific settings are configured in the *Options for PCB Project* dialog, shown below (**Project » Project Options**). The project options include the error checking parameters, a connectivity matrix, Class Generator, the Comparator setup, ECO generation, output paths and connectivity options, Multi-Channel naming formats, Default Print setups, Search Paths, and project-level Parameters. These settings are used when you compile the project.

Project outputs, such as assembly, fabrication outputs and reports can be set up from the **File** and **Reports** menus. These settings are also stored in the Project file so they are always available for this project. An alternate approach is to use an OutputJob file to configure the outputs, with the advantage that an OutputJob can be copied from one project to the next. See More About Outputs to learn more configuring the outputs.

Compiling the Project

After you complete the schematic in Altium Designer, you *compile* it. This generates an internal connectivity map of the design, detailing all of the components and nets. When the project is compiled, comprehensive design and electrical rules are also applied to verify the design. The design and rule checks are configured in the *Options for PCB Project* dialog.

When all errors are resolved, the compiled schematic design is ready to be transferred to the target PCB document by generating a series of Engineering Change Orders (ECOs). Underlying this process is a comparator engine that identifies every difference between the schematic design and the PCB, and generates an ECO to resolve each difference. This approach of using a comparator engine to identify differences means you not only work directly between the schematic and PCB (there is no intermediate netlist file used), it also means the same approach can be used to synchronize the schematic and PCB at any stage during the design process. The comparator engine also allows you to find differences between source and target files and update (synchronize) in both directions. The ECO generation and comparator are also configured in the *Options for PCB Project* dialog.

Checking the Electrical Properties of Your Schematic

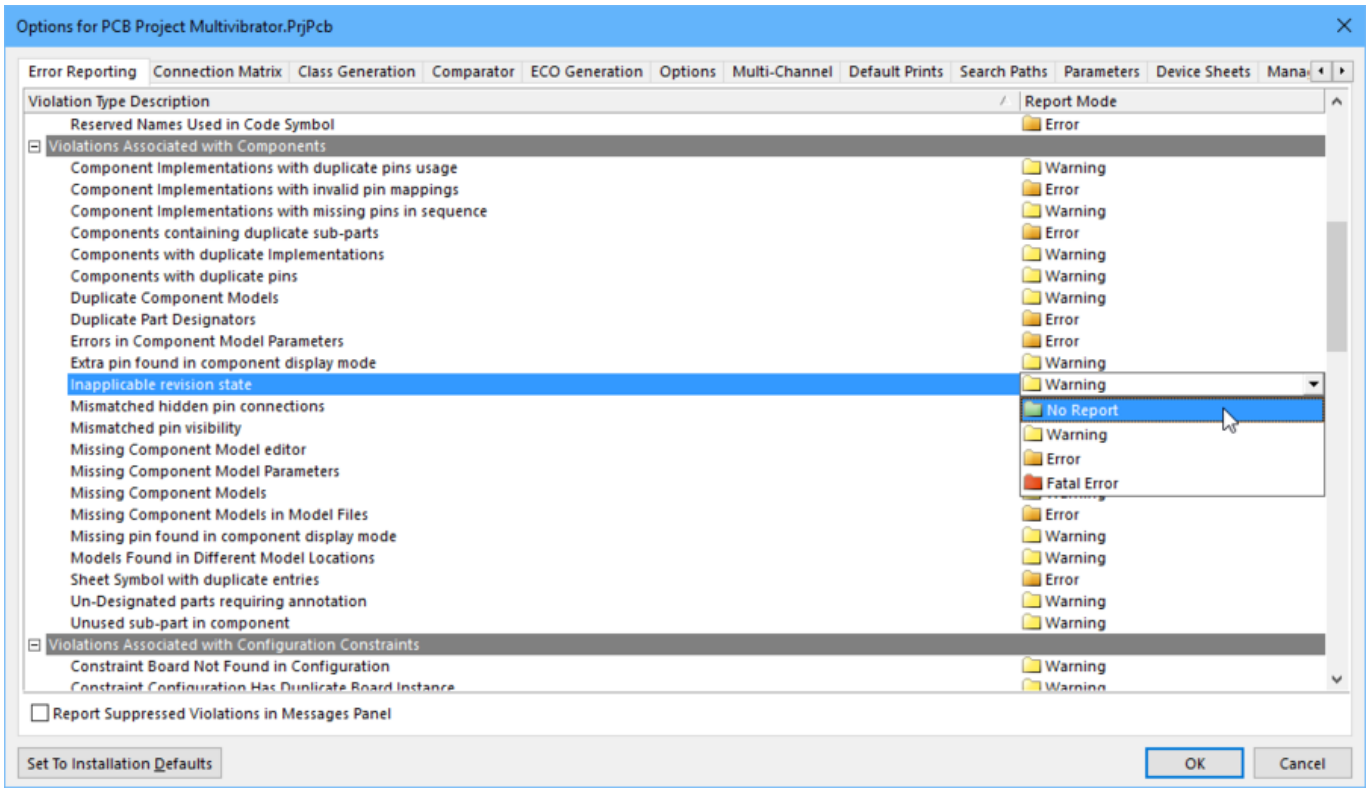
Schematic diagrams are more than just simple drawings - they contain electrical connectivity information about the circuit. You can use this connectivity awareness to verify your design. When you compile a project, the software checks for errors according to the rules set up in the **Error Reporting** and **Connection Matrix** tabs of the *Options for Project* dialog. When you compile the project any violations that are detected will display in the *Messages* panel.

Setting up the Error Reporting

Main article: Error Reporting

The **Error Reporting** tab in the *Options for Project* dialog is used to set up a large range of drafting and component configuration checks. The **Report Mode** settings show the level of severity of a violation. If you wish to change a setting, click on a **Report Mode** next to the violation you wish to change and choose the level of severity from the drop-down list.

For this tutorial there is one check that must be changed. The components in the tutorial have been placed from an Altium Vault, and Vault components support the concept of revisions - where a component can be updated and a new revision released. However, the components in the Altium Content Vault are not revisioned, so will fail the **Inapplicable Revision State** check. For the tutorial, this check must be set to **No Report**, as shown in the image below.



Configure the Error Reporting tab to detect for design errors when the project is compiled.

Configuring the Error Checking:

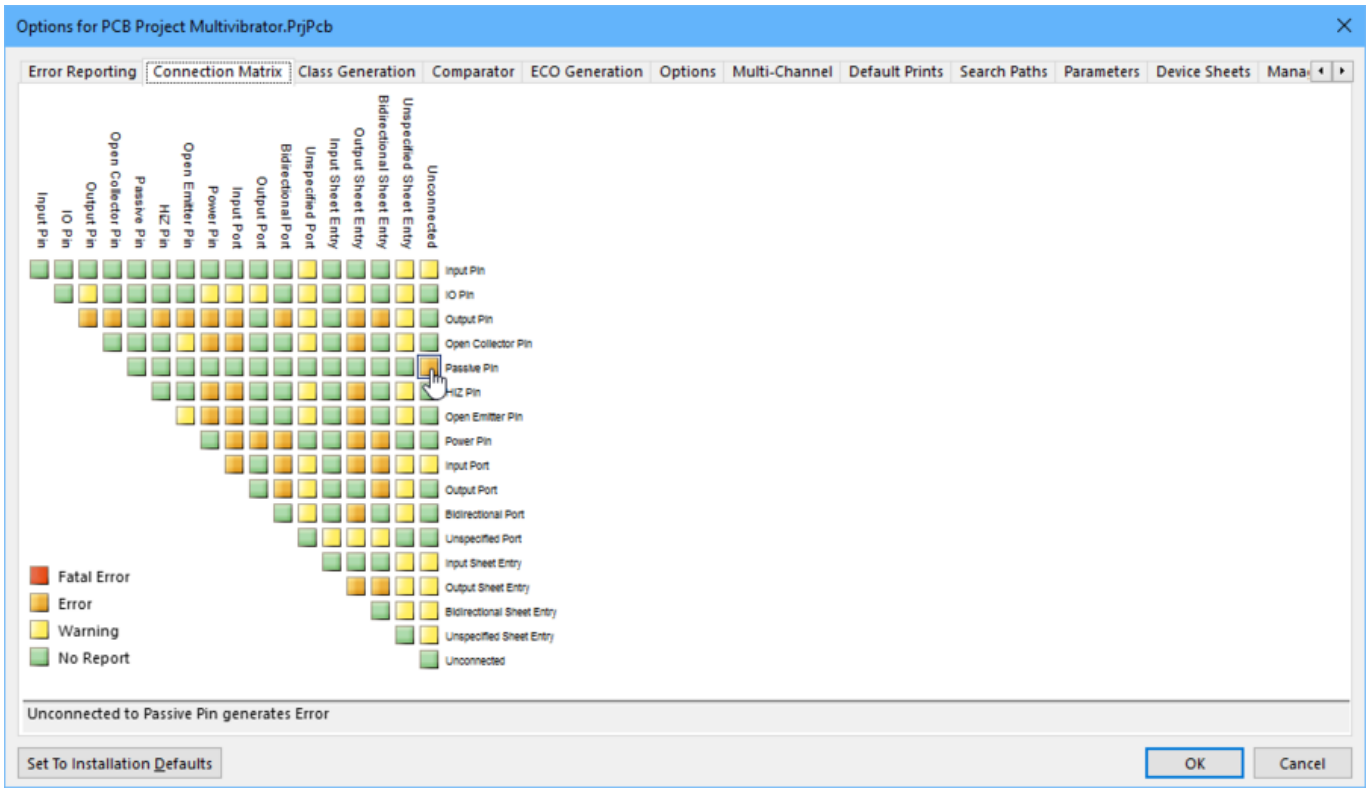
1. Scroll through the list of error checks to the **Violations Associated with Components** group.
2. Locate the **Inapplicable Revision State** check and set it to **No Report**, as shown above.

Setting Up the Connection Matrix

Main article: Connection Martix

When the design is compiled a list of the pins in each net is built in memory. The type of each pin is detected (eg: input, output, passive, etc), and then each net is checked to see if there are pin types that should not be connected to each other, for example an output pin connected to another output pin. The Connection Matrix tab of the **Options for Project** dialog is where you configure what pin types are allowed to connect to each other. For example, look down the entries on the right side of the matrix diagram and find **Output Pin**. Read across this row of the matrix till you get to the **Open Collector Pin** column. The square where they intersect is orange, indicating that an Output Pin connected to an Open Collector Pin on your schematic will generate an error condition when the project is compiled.

You can set each error type with a separate error level, eg. from no report, through to a fatal error. Click on a colored square to change the setting, continue to click to move to the next check-level. Set the matrix so that **Unconnected Passive Pin generates Error**, as shown in the image below.



The Connection Matrix defines what electrical conditions are checked for on the schematic, note that the Unconnected - Passive Pin setting is being changed.

Changing the Connection Matrix:

1. To change one of the settings click the colored box, it will cycle through the 4 possible settings. Note that you can **right-click** on the dialog face to display a menu that lets you toggle all settings simultaneously, including an option to restore them all to their **Default** state (handy if you have been toggling settings and cannot remember their default state).
2. Your circuit contains only Passive Pins (on resistors, capacitors and the connector) and Input Pins (on the transistors). Let's change the default settings so that the connection matrix detects unconnected passive pins. Look down the row labels to find the **Passive Pin** row. Look across the column labels to find **Unconnected**. The square where these entries intersect indicates the error condition when a *passive pin* is found to be *unconnected* in the schematic. The default setting is green, indicating that no report will be generated.

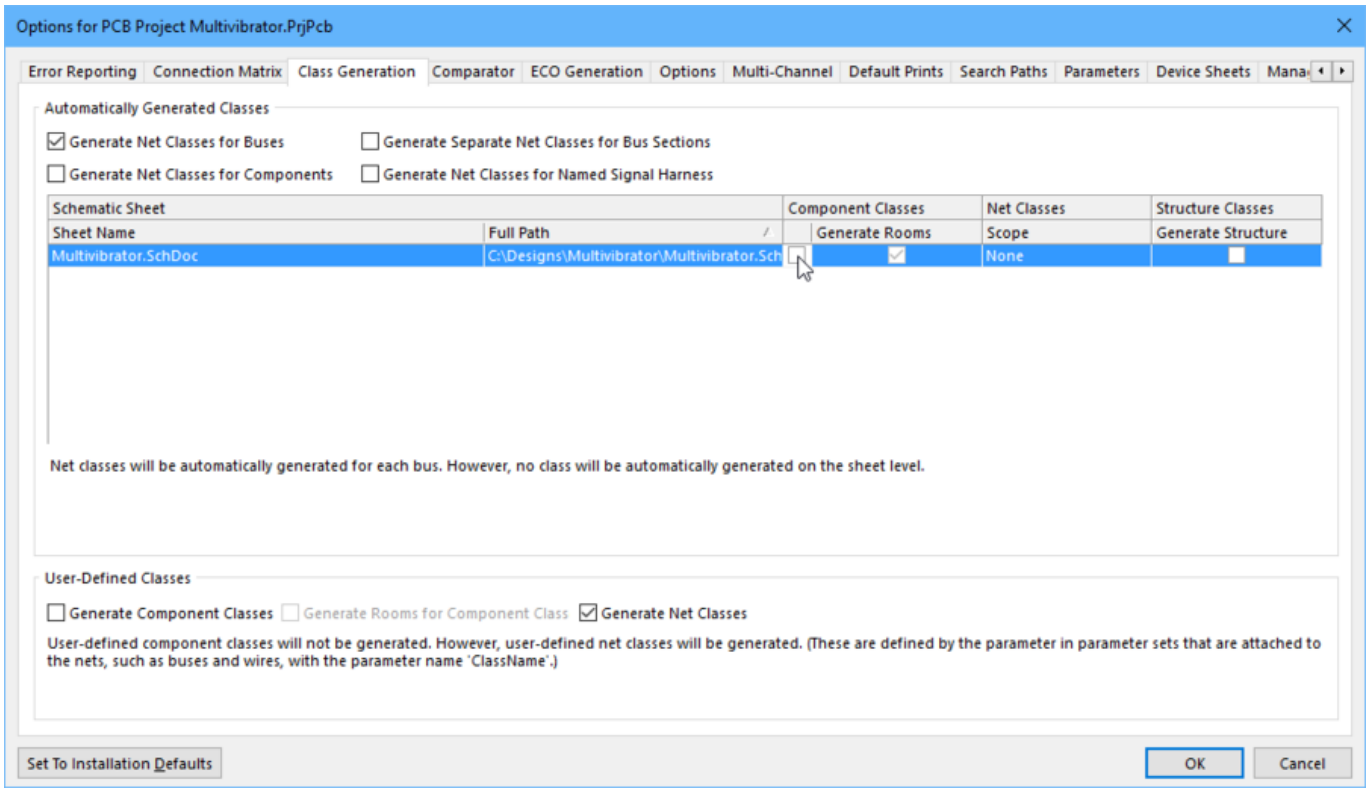
3. Click on this intersection box until it turns Orange (as shown in the image above), so that an error will be generated for unconnected passive pins when the project is compiled. You will purposely create an instance of this error later in the tutorial.

Configuring the Class Generation

Main article: Class Generation

The **Class Generation** tab in the *Options for Project* dialog is used to configure what type of classes are generated from the design (the Comparator and ECO Generation tabs are then used to control if classes are transferred to the PCB). By default, the software will generate Component classes and Rooms for each schematic sheet, and Net Classes for each bus in the design. For a simple, single-sheet design such as this there is no need to generate a component class or a room - ensure that the **Component Classes** checkbox is cleared, doing this will also disable the creation of a room for that component class.

Note that this tab of the dialog also includes options for **User-Defined Classes**.



The Class Generation tab is used to configure what classes and rooms are automatically created for the design.

Configuring Class Generation:

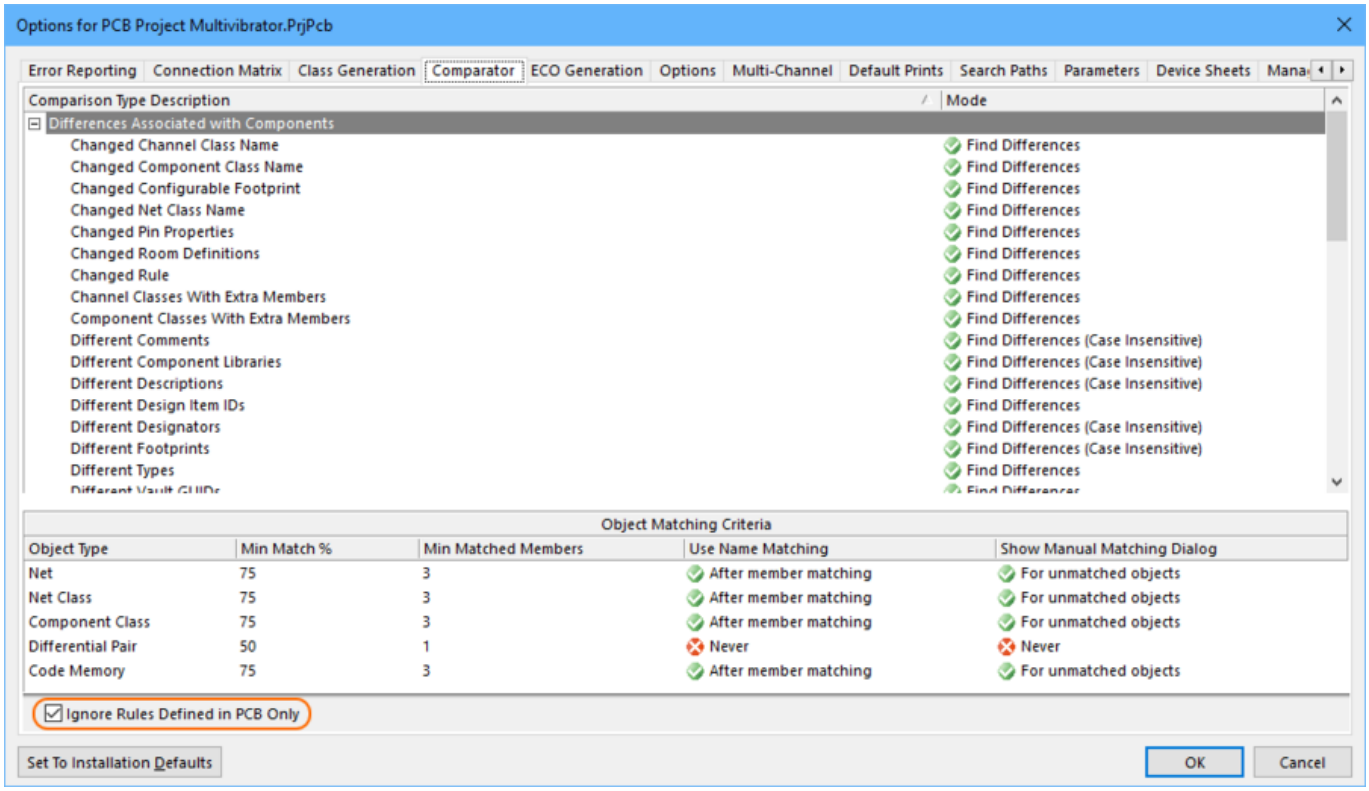
1. Clear the **Component Classes** checkbox, as shown in the image above. This will automatically disable the creation of a placement room for that schematic sheet.
2. There are no buses in the design, so there is no need to clear the **Generate Net Classes for Buses** checkbox located near the top of the dialog tab.
3. There are no user-defined Net Classes in the design (done through the placement of Net Class directives on the wires), so there is no need to clear the **Generate Net Classes** checkbox in the **User-Defined Classes** region of the dialog tab.

Setting Up the Comparator

Main article: Comparator

The Comparator tab in the *Options for Project* dialog sets which differences between files will be reported or ignored when a project is compiled. Generally the only time you will need to change settings in this tab is when you add extra detail to the PCB, such as design rules, and do not want those settings removed during design synchronization. If you need more detailed control, then you can selectively control the comparator using the individual comparison settings.

For this tutorial it is sufficient to confirm that the **Ignore Rules Defined in PCB Only** option is enabled, as shown in the image below.



The Comparator tab is used to configure exactly what differences the comparison engine will check for.

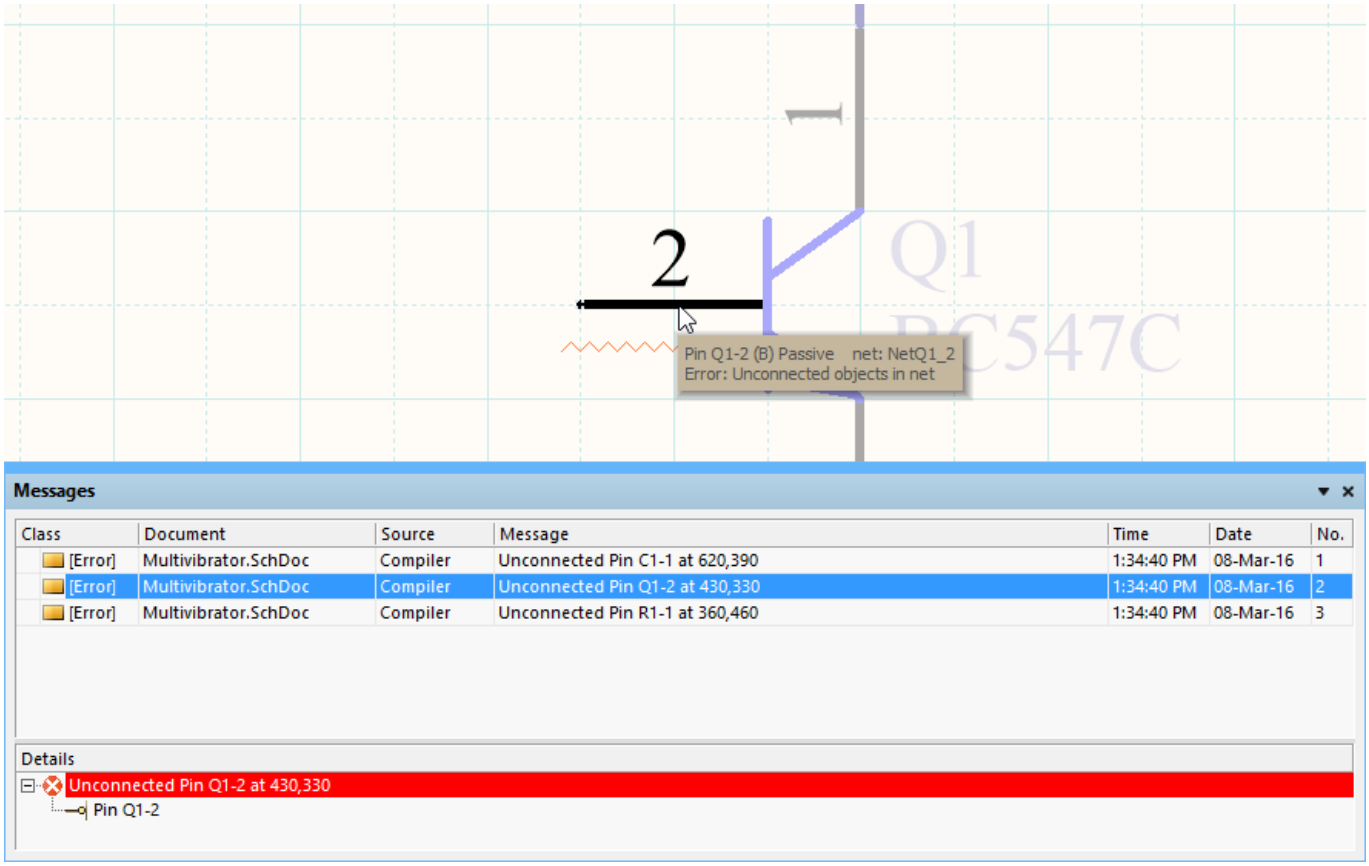
You are now ready to compile the project and check for any errors.

Compiling the Project to Check for Errors

Main article: Compiling and Verifying the Design

Compiling a project checks for drafting and electrical rules errors in the design documents, and details all warnings and errors in the *Messages* panel. You have set up the rules in the **Error Checking** and **Connection Matrix** tabs of the *Options for Project* dialog, so are now ready to check the design.

To compile the project and check for errors, select **Project » Compile PCB Project Multivibrator.PrjPcb**.



Use the Messages panel to locate and resolve design errors - double-click on an error to pan and zoom to that object.

Compiling and checking for errors:

1. To compile the Multivibrator project, select **Project » Compile PCB Project Multivibrator.PrjPcb**.
2. When the project is compiled, all warnings and errors are displayed in the *Messages* panel. The panel will only appear automatically if there are errors detected (not when there are only warnings), to open it manually click the System button down the bottom right, and select **Messages** from the menu.
3. If your circuit is drawn correctly, the *Messages* panel should not contain any errors, just the message *Compile successful, no errors found*. If the there are errors, work through each one, checking your circuit and ensuring that all wiring and connections are correct.

You will now deliberately introduce an error into the circuit and recompile the project:

1. Click on the `Multivibrator.SchDoc` tab at the top of the design window to make the schematic sheet the active document.
2. Click in the middle of the wire that connects R1 to the base wire of Q1. Small, square editing handles will appear at each end of the wire and the selection color will display as a dotted line along the wire to indicate that it is selected. Press the **Delete** key on the keyboard to delete the wire.
3. Recompile the project (**Project » Recompile PCB Project Multivibrator.PrjPcb**) to check for errors. The *Messages* panel will display warning messages indicating you have unconnected pins in your circuit.
4. The *Messages* panel is divided horizontally into 2 regions, as shown in the image above. The upper region lists all messages; which can be saved, copied, cross probed to, or cleared via the **right-click** menu. The lower region details the warning/error currently selected in the upper region of the panel.
5. When you double-click on an error or warning in either region of the *Messages* panel, the

schematic view will pan and zoom to the object in error.

Before you finish this section of the tutorial, let's fix the error in our schematic.

1. Make the schematic sheet the active document.
2. Undo the delete action (**Ctrl+Z**) to restore the deleted wire.
3. To check that there are no longer any errors, recompile the project (**Project » Recompile PCB Project Multivibrator.PrjPcb**) - the *Messages* panel should show no errors.
4. Save the schematic and the project file as well.

When you double click on an error in the *Messages* panel:

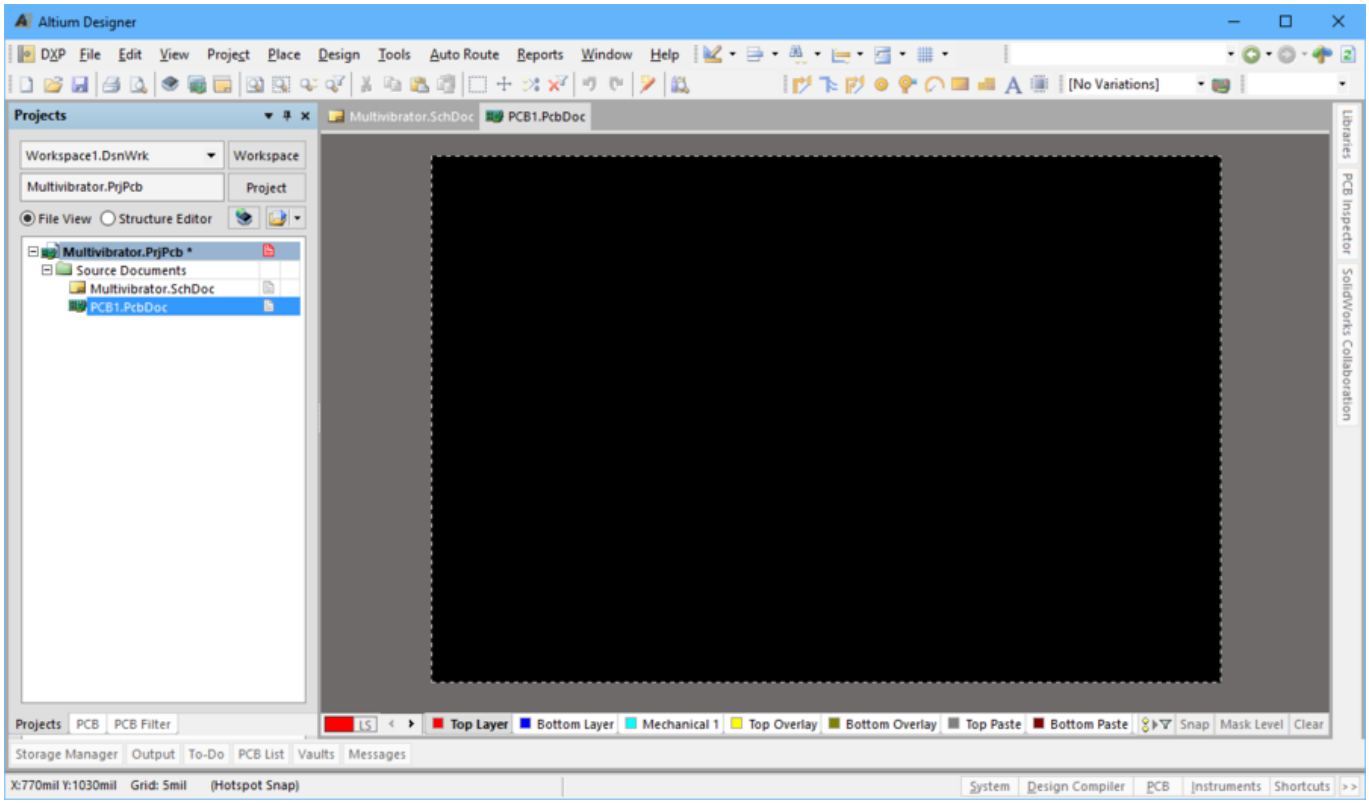
- The entire schematic fades, except for the object in error. The amount that the schematic fades is controlled by the **Dim** level, set by clicking the Mask Level button down the bottom right. Click the Clear button (**Shift+C**) to clear all masking / dimming.
- The schematic zooms to present the object in error. The **Zoom Precision** is set in the **System - Navigation** page of the *Preferences* dialog.

To clear all messages from the *Messages* panel, **right-click** in the panel and select **Clear All**.

Schematic capture is now complete, time to create the PCB!

Creating a New PCB

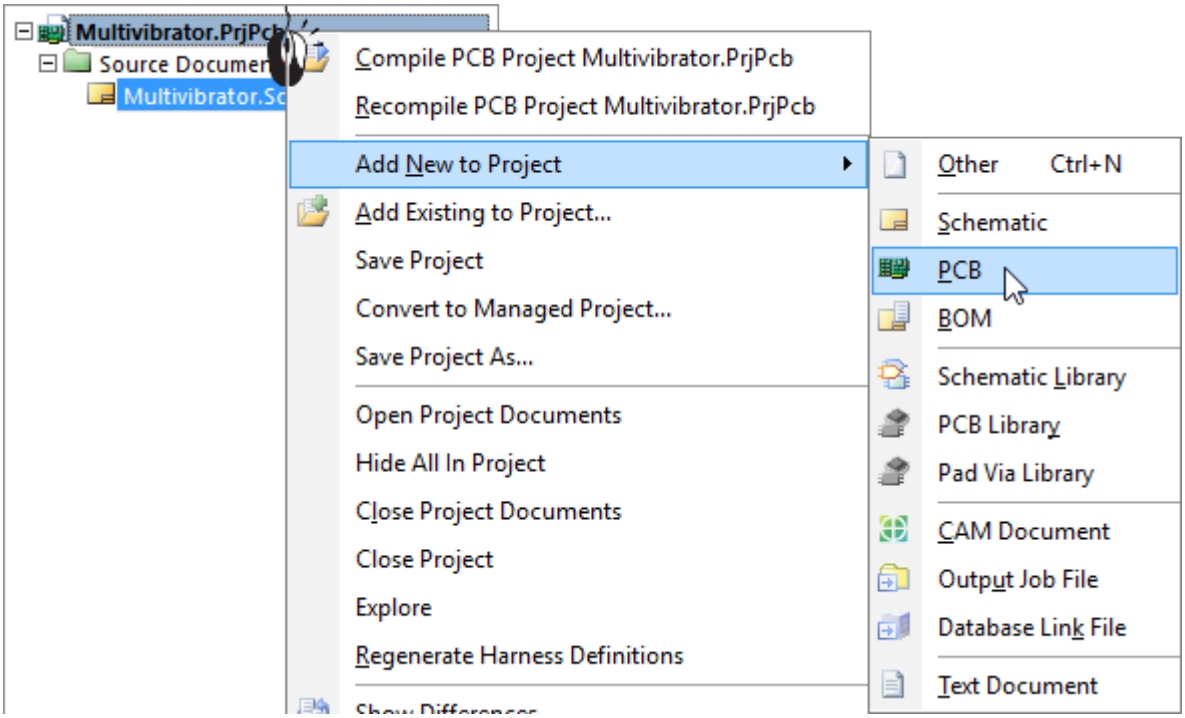
Before you transfer the design from the Schematic Editor to the PCB Editor, you need to create the blank PCB, then name and save it as part of the project.



The blank PCB has been added to the project.

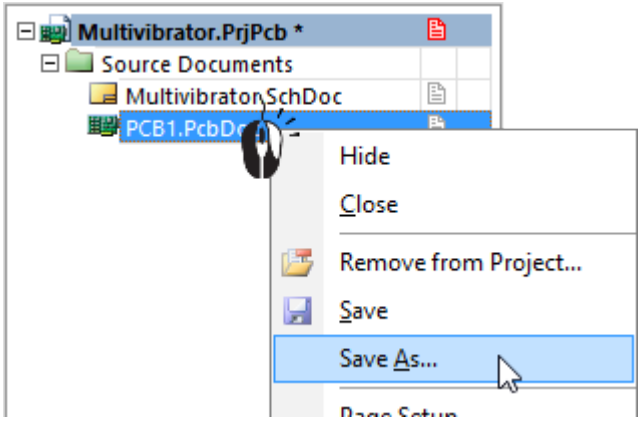
[Adding a New Board to the Project:]

1. A new PCB can be added to the project via the *Projects* panel right-click menu, select the **Add New to Project » PCB** command.



Add a new PCB to your project.

2. The PCB will appear as a Source Document in the Project, as shown below. **Right-click** on the PCB icon in the *Projects* panel to select the **Save As** command, naming it `Multivibrator`. Note that you do not need to enter the file extension in the *Save As* dialog, this is automatically appended.



Save the PCB file with a meaningful name.

3. Adding the PCB has changed the project, so save the project too (**right-click** on the project filename in the *Projects* panel, and select **Save Project**).

Configuring the Board Shape and Location

Main article: The Board

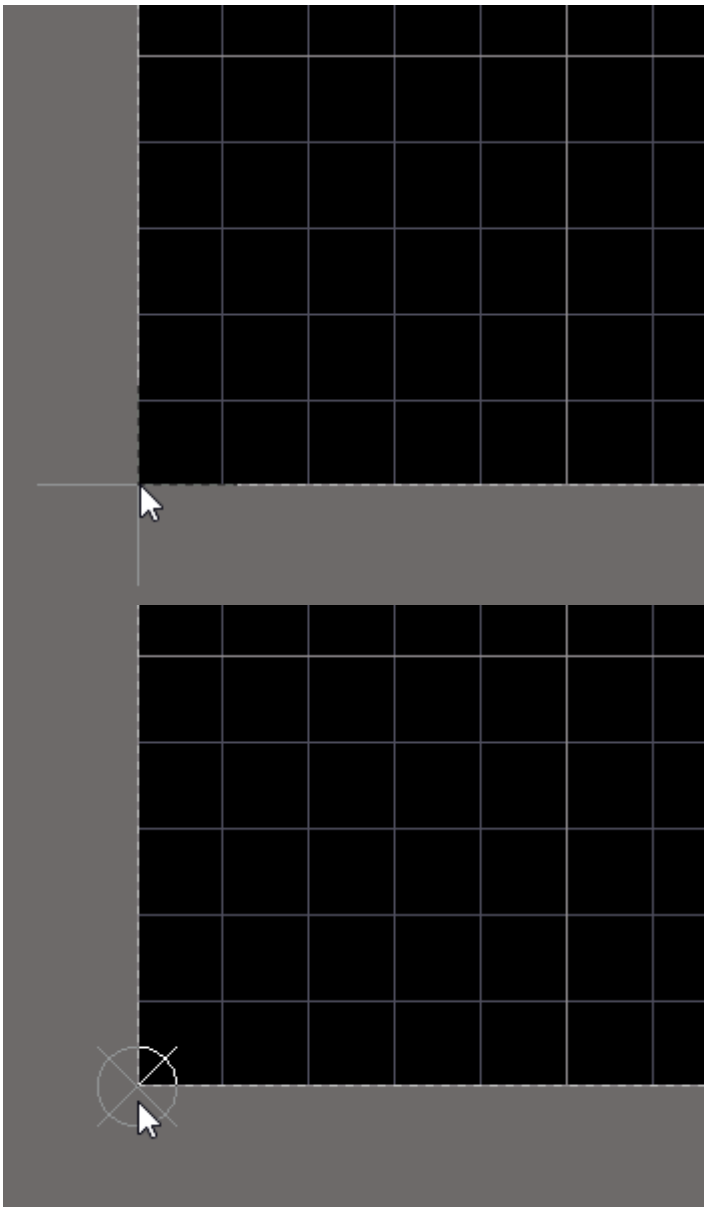
There are a number of attributes of this blank board that need to be changed before transferring the design from the schematic editor, including:

Task	Process
Setting the origin	The PCB editor has two origins, the Absolute Origin, which is the lower left of the workspace, and the user-definable Relative Origin, which is used to determine the current workspace location - the coordinates shown on the Status bar are relative to this origin. A common approach is to set the Relative Origin to the lower-left corner of the board shape. Select the **Edit » Origin » Set** command to set the Relative Origin, use the **Reset** command to reset it back to the Absolute Origin.
Change from Imperial to Metric units	The current workspace X / Y location and Grid are displayed on the Status bar, which is displayed along the bottom of the software. For this tutorial metric units will be used - to change the units, either press **Q** on the keyboard to toggle back and forth between Imperial and Metric units, or select the **View » Toggle Units** command from the menus. You can also force a change of units if you enter the units with a grid value in the *Snap Grid* dialog.
Selecting a suitable snap grid	You will have noticed that the current snap grid is 0.127mm, which is the old 5mil imperial snap grid, converted to metric. To change the snap grid at any time, right-click in the workspace and select the **Snap Grid** submenu, where you can select an imperial or metric value. Note the shortcuts shown in the menu, use **Ctrl+Shift+G** to open the *Snap Grid* dialog, which is handy when you want to type in a specific value. Other useful shortcuts include **G** to display the Snap Grid submenu, and **Ctrl+G** to open the *Cartesian Grid* editor. Grids are discussed in more detail later in the tutorial.
Redefining the board shape to the required size	The board shape is shown by the black region with a grid in it. The default size for a new board is 6x4 inches, the tutorial board is 30mm x 30mm. Details for the process of defining a new shape for the board are available below.
Configuring the layers used in the design	As well as the copper, or electrical layers you route on, there are also general-purpose mechanical layers, and special-purpose layers such as the component overlays (silkscreens), solder mask, paste mask, and so on. The electrical and other layers will be configured shortly.

Press **Ctrl+PgDn** at any time to zoom to show the entire board.

Setting the Origin and the Grid:

1. There are two origins used in the software, the Absolute Origin, which is the lower left of the workspace, and the user-definable Relative Origin, which is used to determine the current workspace location. Before setting the origin, Keep zooming in to the lower left of the current board shape until you can easily see the grid - to do this position, the cursor over the lower-left corner of the board shape and press **PgUp** until both the Coarse and Fine grids are visible, as shown in the images below.
2. To set the Relative Origin, select **Edit » Origin » Set**, position the cursor over the bottom left corner of the board shape, then **left click** to locate it.

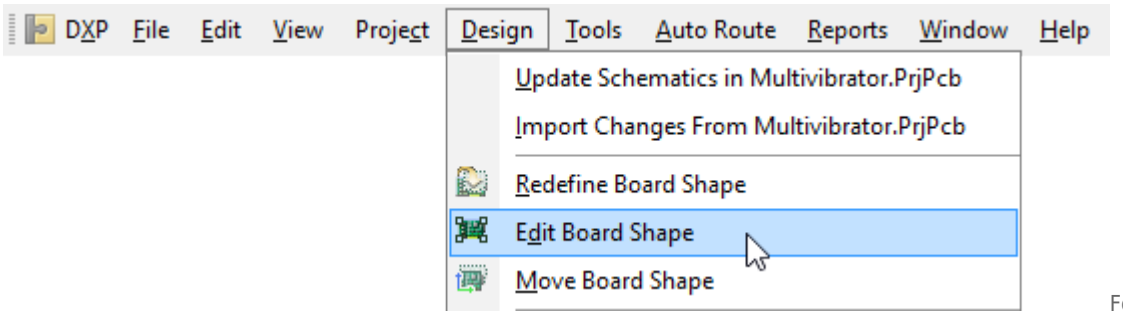


Select the command, position the cursor over the lower-left corner of the board shape (left image), then click to define the origin (right image).

3. The next step is to select a suitable snap grid, as discussed in the table above. During the course of design it is quite common to change grids, for example you might use a coarse grid during component placement, and a finer grid for routing. For this tutorial you will be using a Metric grid. A coarse 5mm grid will be suitable for component placement, press **Ctrl+Shift+G** to open the *Snap Grid* dialog and enter 5mm, then click **OK** to close the dialog.
4. By entering the units as you entered a value, you have also instructed the software to switch to a Metric grid. If you look at the Status bar you can confirm that the Grid is now metric.

Redefining the Board Shape:

1. The default board shape is 6x4 inch, for the tutorial the board size is 30mm x 30mm.
2. To zoom back out and show all of the board, select **View » Fit Board** from the menus (**Ctrl+PgDn**).
3. The board will exactly fill the PCB editor. To manipulate the size you need to be able to see the edges of the board, use **Ctrl+WheelRoll** to zoom out a bit more, or press **PgDn**.
4. The next step is to change the board shape. To do this you must be in Board Planning Mode, select **View » Board Planning Mode** to change (shortcut: **1**). The display will change, the board area will now be shown in green.
5. Your choice now is to either redefine the board shape (draw it again), or edit the existing board shape. For a simple square or rectangle, it is more efficient to edit the existing board shape, to do this select **Design » Edit Board Shape** from the menus. Note that you must be in Board Planning Mode for this command to be available.



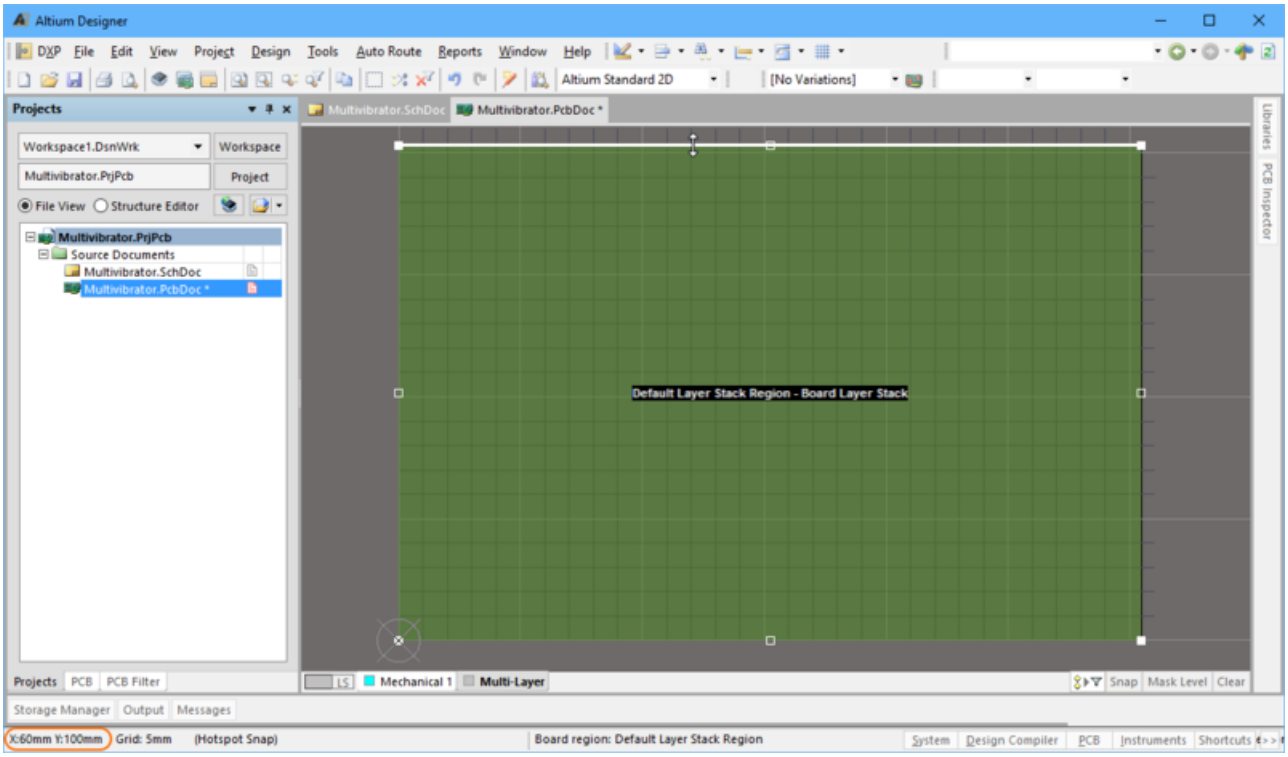
For this design, it is more efficient to edit the existing board shape. These commands are only available in Board Planning Mode.

6. Editing handles will appear at each corner and the center of each edge, as shown below.

> Note that clicking anywhere other than on an editing handle or an edge of the shape will drop you out of board shape editing mode.

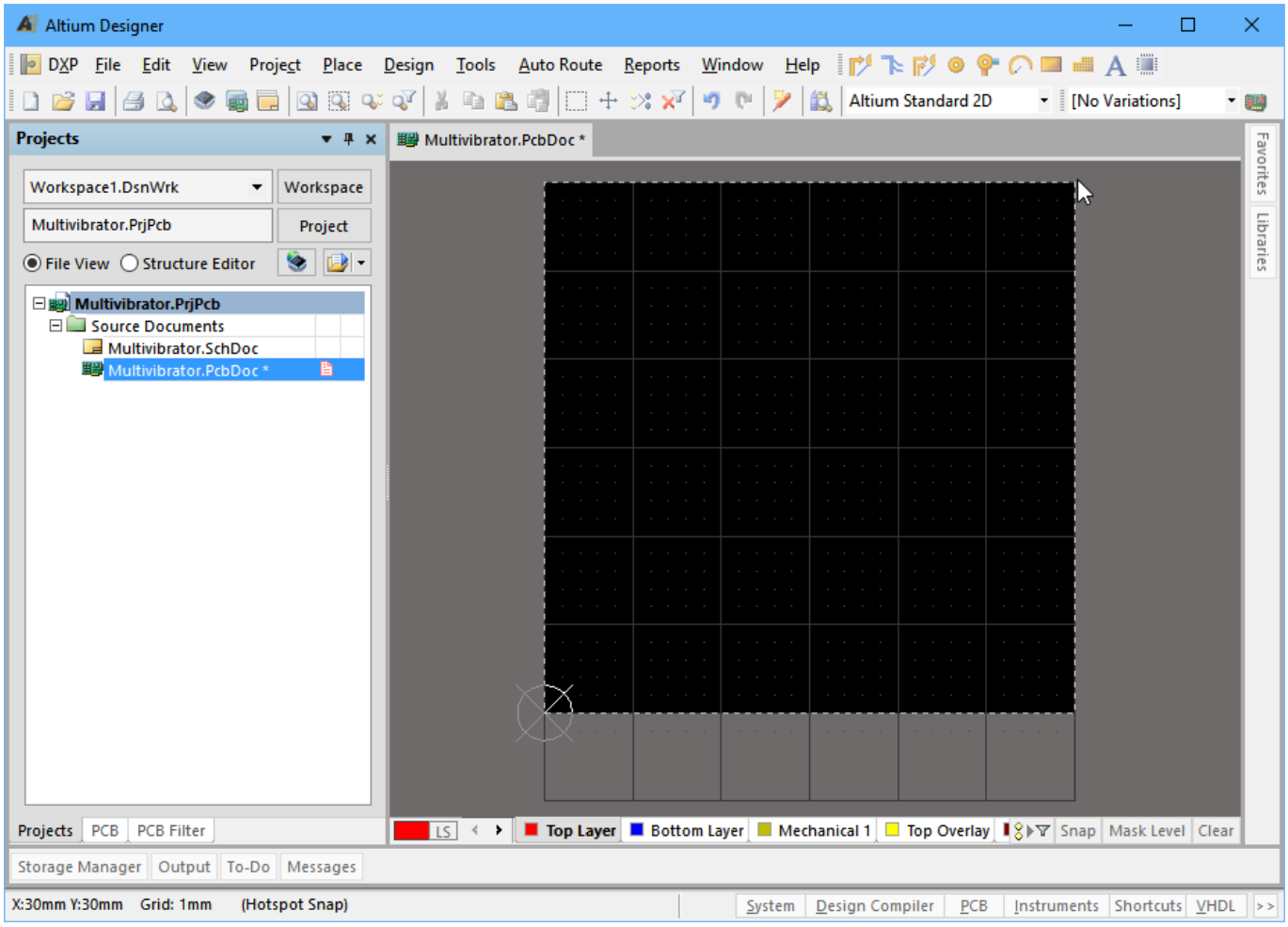
7. The objective is to resize the shape to create a 30mm by 30mm board. The Coarse visible grid is 25mm (5x the snap grid), and the Fine visible grid is 5mm - these can be used as a guide. You can now either: slide the upper edge down and the right edge in to create the correct size; or move 3 of the corners in, leaving the one that is at the origin in its current location.
8. To slide the upper edge down, position the cursor over the edge (but not over a handle), when the cursor changes to a double-headed arrow click and hold, then drag the edge to the new location so that the Y cursor location is 30mm on the Status bar, as shown in the image below.
9. Repeat the process to move the right-hand edge in, positioning it when the X cursor location is 30mm on the Status bar.

> Use the current location information down the bottom left of the Status bar to guide you as you reshape the board.



The resize cursor is shown, use the location information on the Status bar to help you resize the board to 30mm x 30mm.

8. Click anywhere in the workspace to drop out of board shape editing mode.
9. Press the **2** shortcut to switch back to 2D Layout Mode.
10. Now that the shape has been defined you can set the grid to a value suitable for component placement, for example 1mm. Grids are discussed in detail shortly.
11. Save the board.



The board size has been defined, and the units, origin and grid have been set. The required layers will be configured shortly.

A good approach to defining the shape of a non-rectangular board is to place a series of tracks (and arcs for curved boards) on the keepout layer. As well as being useful as a placement and routing keep-away barrier, these tracks and arcs can be selected (**Edit » Select » All on Layer**) and used to create the board shape using the **Design » Board Shape » Define from Selected Objects** command.

Transferring the Design

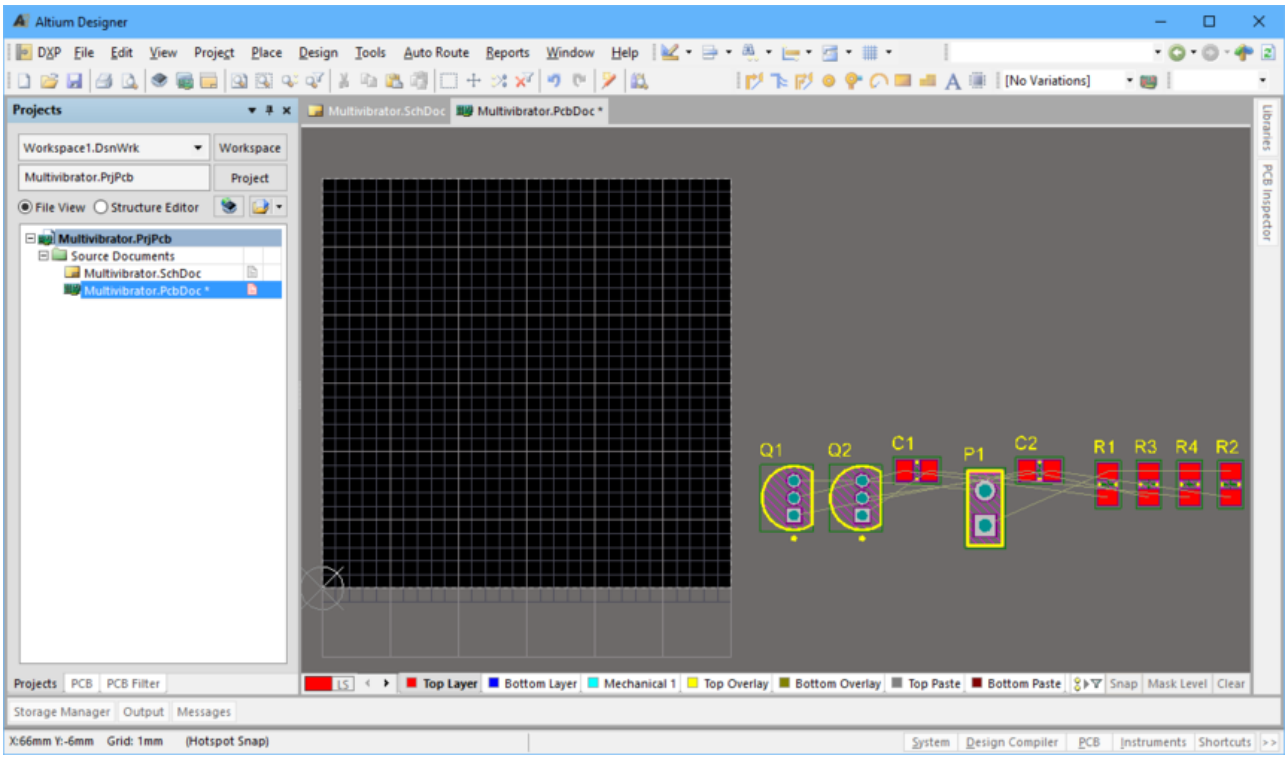
Main article: Working Between the Schematic and the Board

The design is transferred directly between the schematic editor and the PCB editor, there is no intermediate netlist file created. From the schematic editor you select **Design » Update PCB Document Multivibrator.PcbDoc**, or from the PCB editor you select **Design » Import Changes from Multivibrator.PrjPcb**.

When you run either of these commands the design is compiled and a set of Engineering Change Orders is created, which:

- List all components used in the design, and the footprint required for each. When the ECOs are executed the software will attempt to locate each footprint in the currently available libraries or available Content Vault, and place each into the PCB workspace. If the footprint is not available, an error will occur.

- A list of all nets (connected component pins) in the design is created. When the ECOs are executed the software will add each net to the PCB, and then attempt to add the pins that belong to each net. If a pin cannot be added an error will occur - this most often happens when the footprint was not found, or the pads on the footprint do not map to the pins on the symbol.
- Additional design data is then transferred, such as net and component classes.



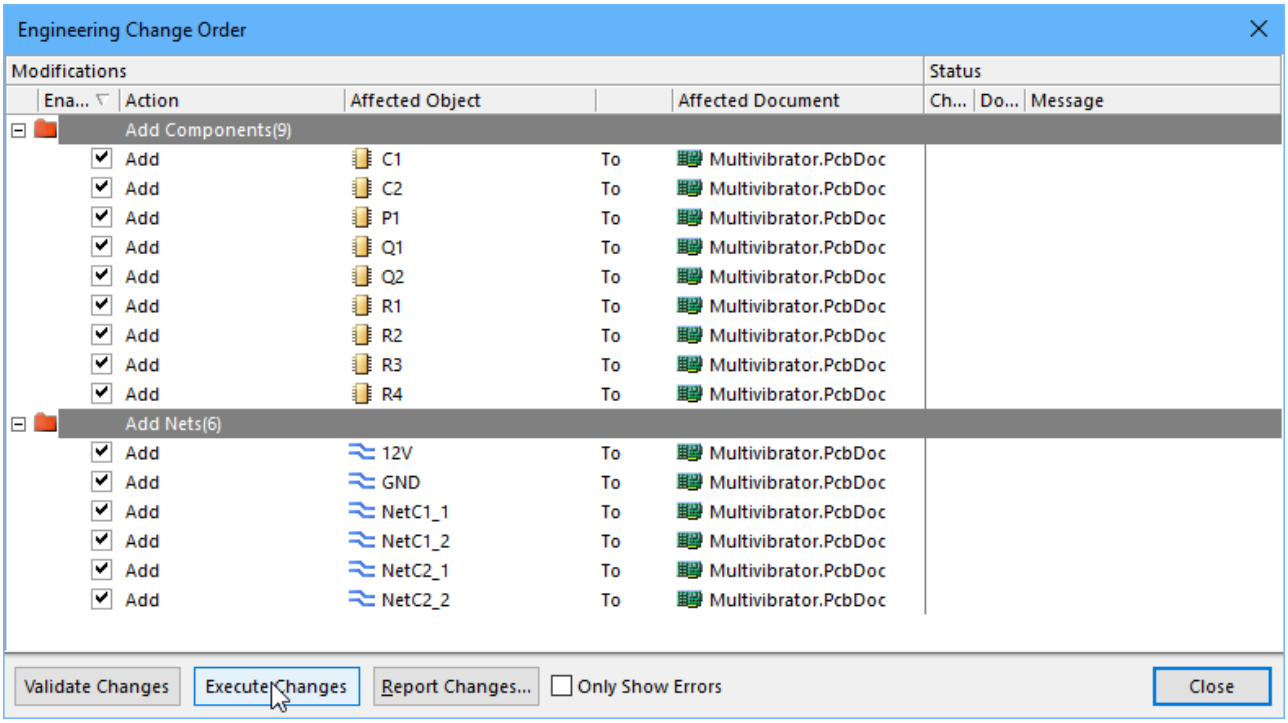
Once the ECOs have been executed, the components are placed outside the board shape and the nets are created.

Before transferring the schematic information to the new blank PCB, make sure all the related libraries for both schematic and PCB are available. Since only the Altium Content Vault is used in this tutorial, the required Vault is already available. As the Vault includes the symbol and the footprint, then the footprints required for the tutorial are also available.

The default settings for all of the PCB objects can be defined in the **PCB Editor - Defaults** page of the *Preferences* dialog. For example, if you want the component designators for all of your PCB designs to be 1.5mm high Arial Truetype, edit the Component defaults.

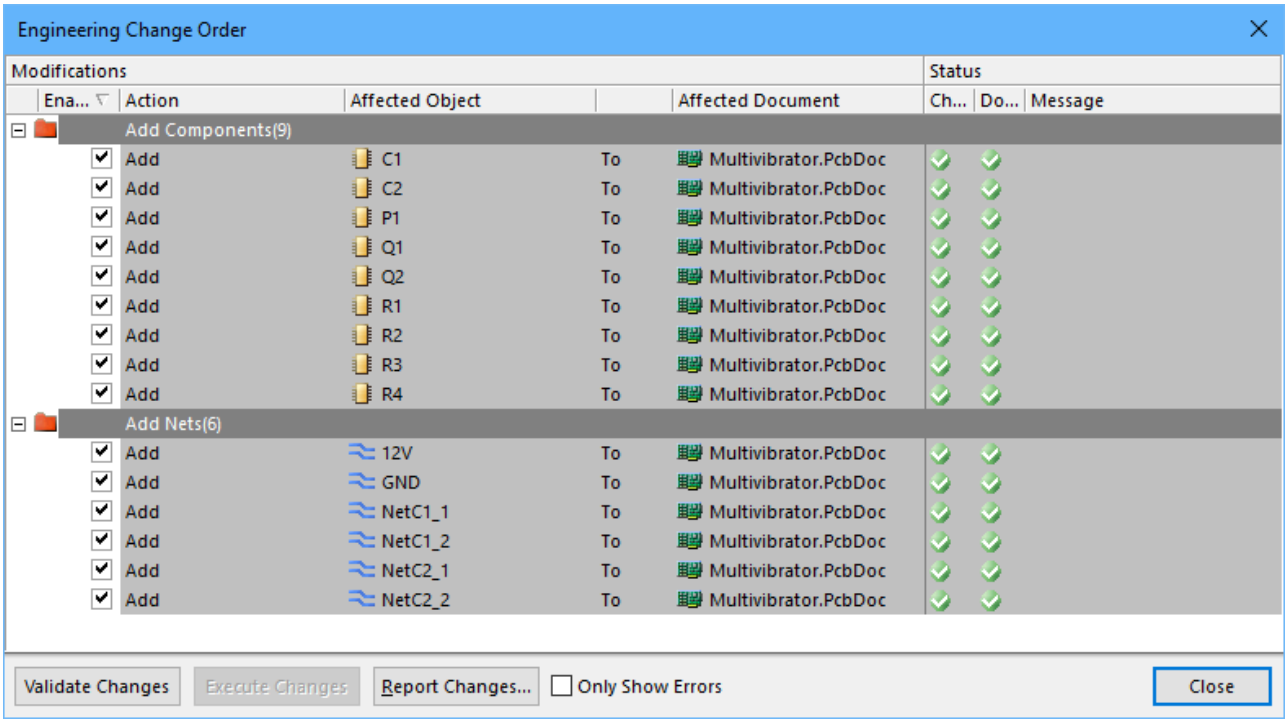
Transferring the design from schematic capture to PCB layout:

1. Make the schematic document, Multivibrator.SchDoc, the active document.
2. Select **Design » Update PCB Document Multivibrator.PcbDoc** from the Schematic editor menus. The project will compile and the *Engineering Change Order* dialog will open.



An ECO is created for each change that needs to be made to the PCB so that it matches the schematic.

3. Click on **Validate Changes**. If all changes are validated, a green tick will appear next to each change in the **Status** list. If the changes are not validated, close the dialog, check the *Messages* panel and resolve any errors.
4. If all changes are validated, click on **Execute Changes** to send the changes to the PCB editor.
5. When completed, the target PCB opens with the *Engineering Change Order* dialog open on top of it, and the **Done** column entries become ticked (as shown in the image below).
6. Click to **Close** the dialog and complete the transfer process.



7. The components will have been positioned outside of the board, ready for placing on the board. There are a few steps before starting the component process, such as configuring the placement grid, the layers and the design rules.

> You can create a report of the ECOs by clicking the **Report Changes** button.

Setting Up the PCB Workspace

Once all of the ECOs have been executed the components and nets will appear in the PCB workspace, just to the right of the board outline, as shown in the image above.

Before you start positioning the components on the board you need to configure certain PCB workspace and board settings, such as the layers, grids and design rules.

Configuring the Display of Layers

Main article: View Configurations

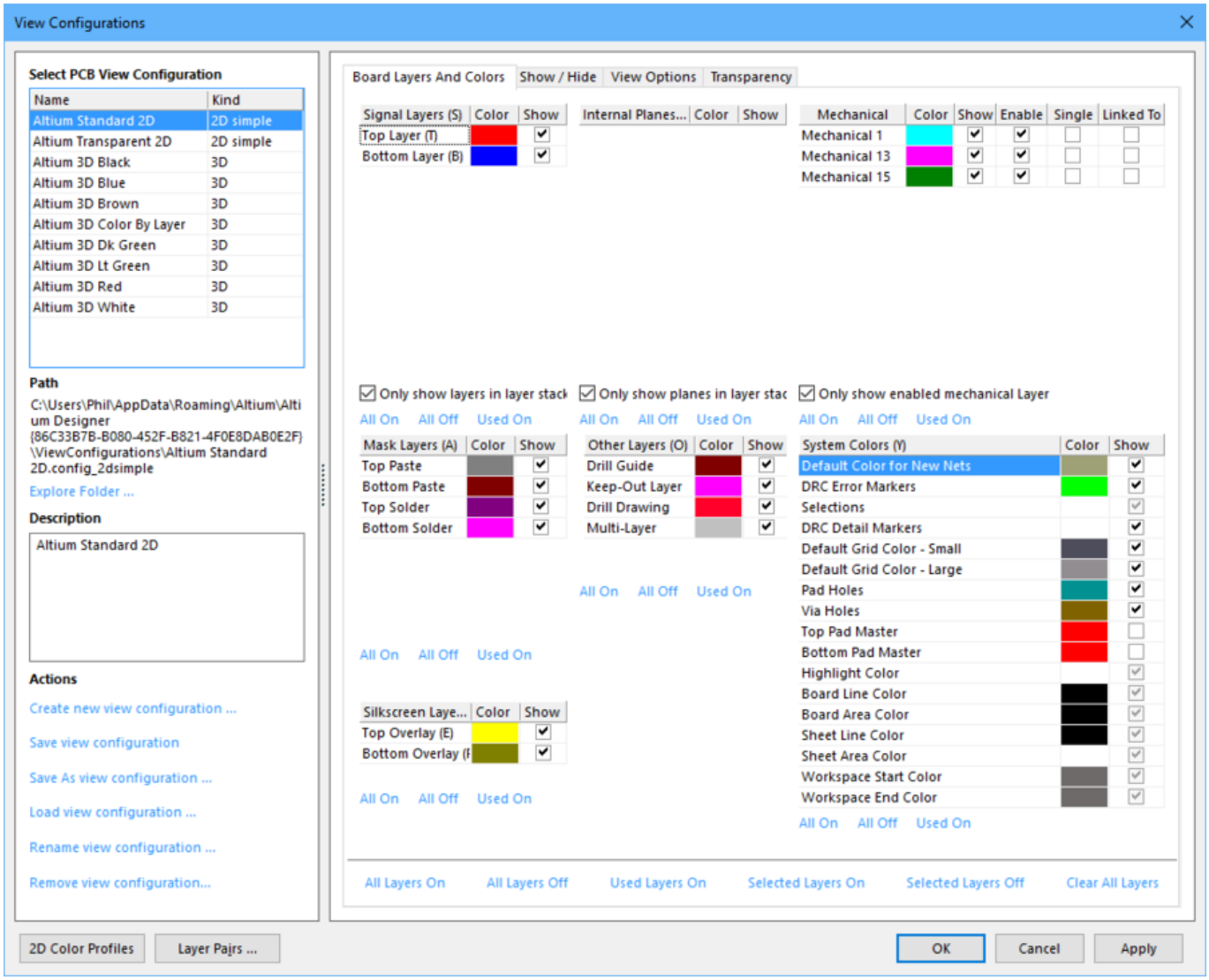
As well as the the layers used to fabricate the board, including: signal, power plane, mask and silkscreen layers, the PCB Editor also supports numerous other non-electrical layers. The layers are often grouped in the following way:

- **Electrical layers** - includes the 32 signal layers and 16 internal power plane layers.
- **Mechanical layers** - there are 32 general purpose mechanical layers, used for design tasks such as dimensions, fabrication details, assembly instructions, or special purpose tasks such as glue dot layers. These layers can be selectively included in print and Gerber output generation. They can also be paired, meaning that objects placed on one of the paired layers in the library editor, will flip to the other layer in the pair when the component is flipped to the bottom side of the board.
- **Special layers** - these include the top and bottom silkscreen layers, the solder and paste mask layers, drill layers, the Keep-Out layer (used to define the electrical boundaries), the multilayer

(used for objects present on all signal layers, such as pads and vias), the connection layer, DRC error layer, grid layers, hole layers, and other display-type layers.

The display attributes of all layers are configured in the *View Configurations* dialog. To open the dialog:

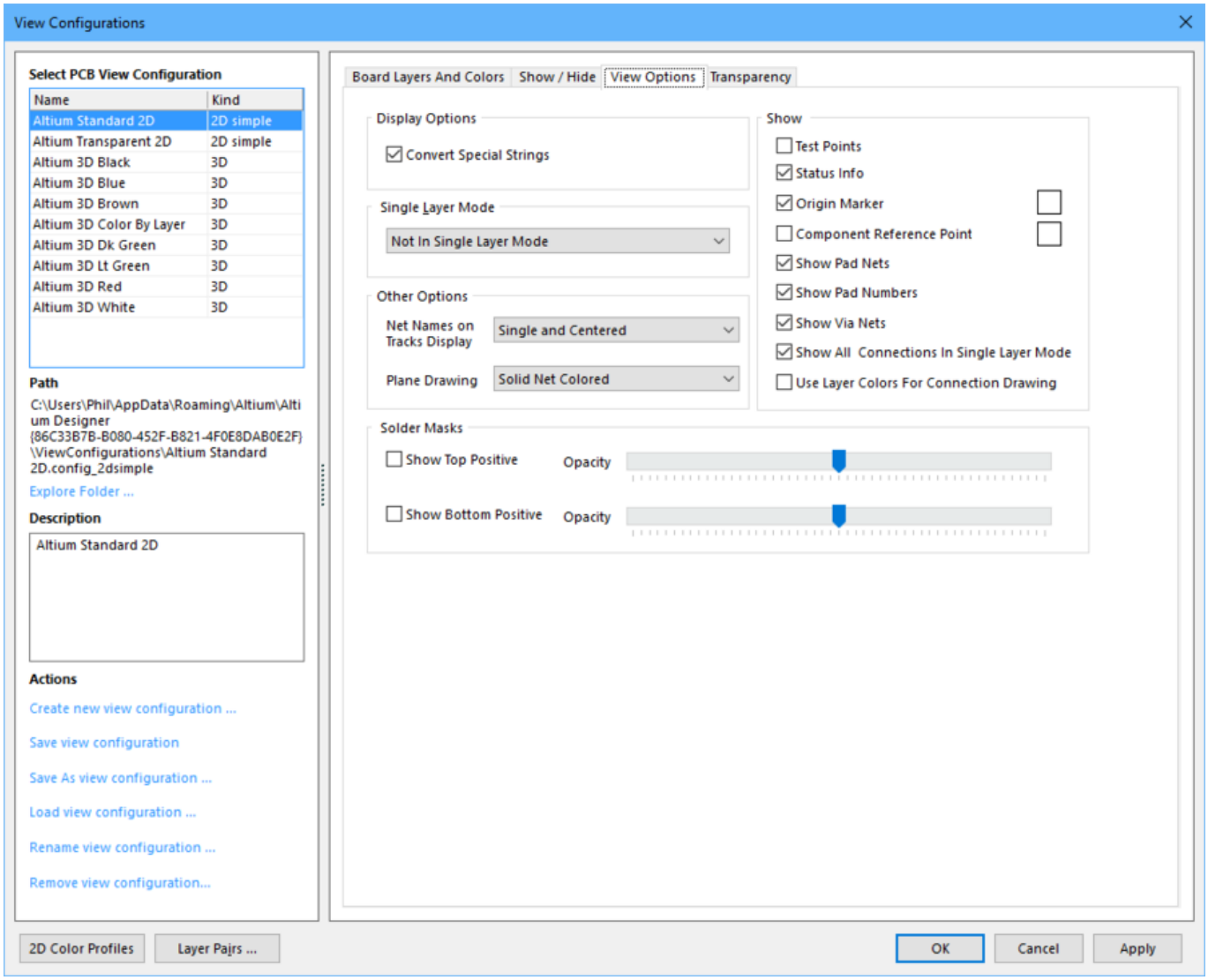
- Select the **Design » Board Layers and Colors** menu entry, or
- Press the **L** shortcut, or
- Click the current layer color  icon down the bottom-left of the workspace.



Press the L shortcut to open the View Configurations dialog.

As well as the layer display state and color settings, the *View Configurations* dialog also gives access to other display settings, including:

- How each type of object is displayed (solid, draft or hidden), in the **Show/Hide** tab of the dialog.
- Various view options, such as if **Pad Net** names and **Pad Numbers** are to be displayed, the **Origin Marker**, if **Special Strings** should be converted, and so on. These are configured in the **View Options** tab of the dialog.



Configure other view options, such as the display of net names on pads and tracks.

Layer Tips

- The currently enabled layers are shown as a series of Tabs across the bottom of the PCB workspace. Right-click on a Tab to access frequently-used layer display commands.
- In a busy design, it can help to only display the layer currently being worked on - to toggle the display in/out of single layer mode press the **Shift+S** shortcut. The **Available Single Layer Modes** are configured in the **PCB Editor - Board Insight Display** page of the *Preferences* dialog.
- To switch the active layer:
  - click the layer Tab, or
  - press the **+** or **-** numeric keys to cycle through all layers, or
  - press the * numeric key to cycle through signal layers, or
  - use the **Ctrl+Shift+WheelRoll** shortcuts.

Configuring the Layer Visibility:

1. Open the *View Configurations* dialog.
2. In the **Board Layers and Colors** tab, confirm that the 2 signal layers are visible.
3. Note that this dialog is where you control the display of the mask layers, the silkscreen layers and the system layers, such as DRC and grids.
4. To have less visual "clutter" during placement and routing, disable the display of the Mechanical Layers, all of the Mask Layers, and the Drill Guide and Drill Drawing layers.
5. Switch to the **View Options** tab.
6. Confirm that the **Show Pad Nets** option is enabled, and the **Net Names on Tracks Display** is set to `Single and Centered`.
7. Click **OK** to accept the settings and close the dialog.

Physical Layers and the Layer Stack Manager

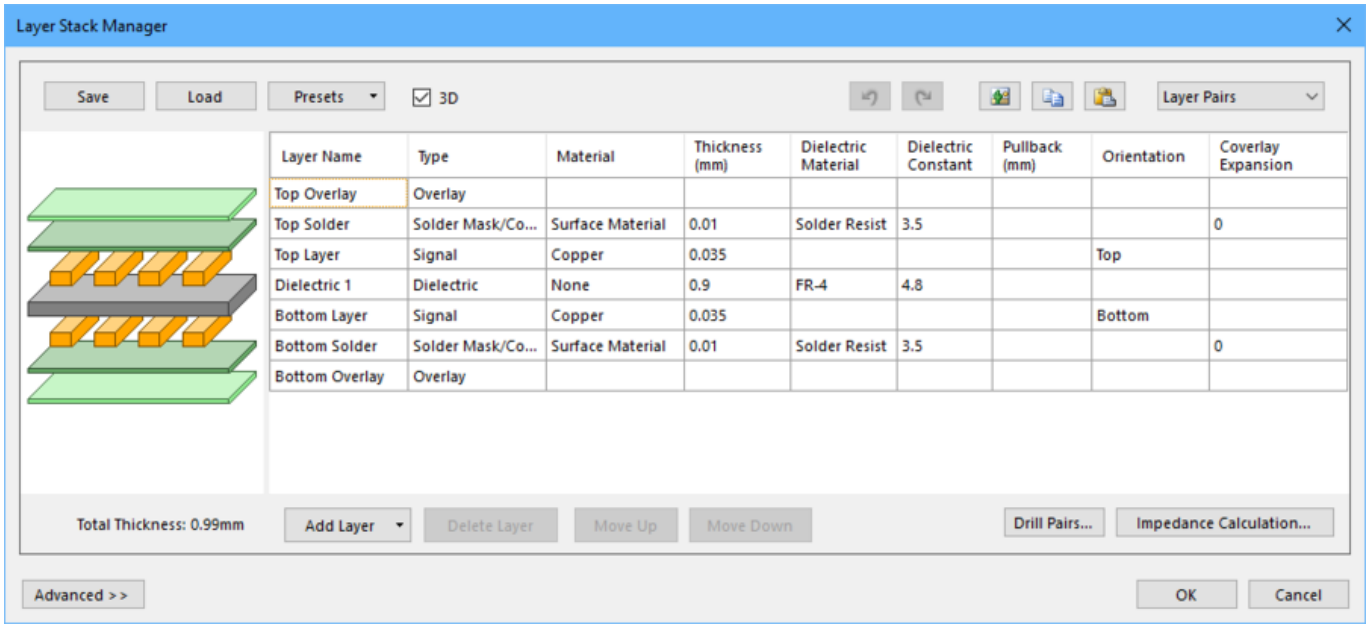
Main article: Layer Stack Manager

As well as the signal and power plane (solid copper) layers, the PCB Editor also includes soldermask and silkscreen physical layers - these are all fabricated to make the physical board. The arrangement of these layers is referred to as the *Layer Stack*. The layer stack is configured in the *Layer Stack Manager*, click **Design » Layer Stack** to open the dialog.

The *Layer Stack Manager* dialog is used to:

- Add / remove signal and power plane layers.
- Add / remove dielectric layers.
- Change the order of the layers.
- Configure the **Material** type for the physical layers.
- Set the layer **Thickness**, **Dielectric Material** and **Dielectric Constant**.
- Define the **Pullback** amount (clearance from plane edge to board edge) for plane layers.
- Define the **Coverlay Expansion** for cover layers.
- Define the component orientation for that layer (advanced feature available in certain Altium products).

The tutorial PCB is a simple design and can be routed as a single-sided or double-sided board. The layer thicknesses shown below have been edited to use sensible metric values.



The properties of the physical layers are defined in the Layer Stack Manager.

To edit a cell either: double-click in the cell; or select the cell and press F2 to show the dropdown or edit the value.

Configuring the board layer stack:

1. Open the *Layer Stack Manager*. For a new board, the default stack comprises: a dielectric core, 2 copper layers, as well as the top and bottom soldermask (coverlay) and overlay (silkscreen) layers, as shown in the image above.
2. New layers and planes are added below the currently selected layer, which is done via the **Add Layer** button, or the right-click menu.
3. Layer properties, such as material, copper thickness and dielectric properties, are included when a **Layer Stack Table** is placed, and are also used for signal integrity analysis. Double-click in a cell to configure that setting. For example, the **Thickness** settings shown in the image below have been changed slightly to more suitable metric values.
4. When you have finished exploring the layer stack options, restore the values to those shown in the image above and click **OK** to close the dialog.

Imperial or Metric Grid?

The next step is to select a grid that is suitable for placing and routing the components. All the objects placed in the PCB workspace are placed on the current snap grid.

Traditionally, the grid was selected to suit the component pin pitch and the routing technology that you planned to use for the board - that is, how wide do the tracks need to be, and what clearance is needed between tracks. The basic idea is to have both the tracks and clearances as wide as possible, to lower the fabriction costs and improve the reliability. Of course the selection of track/clearance is ultimately driven by what can be achieved on each design, which comes down to how tightly the components and routing must be packed to get the board placed and routed.

Over time, components and their pins have dramatically shrunk in size, as has the spacing of their pins. The component dimensions and the spacing of their pins has moved from being predominantly imperial with thru-hole pins, to being more-often metric dimensions with surface mount pins. If you are starting out a new board design, unless there is a strong reason, such as designing a replacement board to fit into an existing (imperial) product, you are better off working in metric.

Why?

Because the older, imperial components have big pins with lots of room between them. On the other hand, the small, surface mount devices are built using metric measurements - they are the ones that need a high level of accuracy to ensure that the fabricated/assembled/functional product works, and is reliable. Also, the PCB editor can easily handle routing to off-grid pins, so working with imperial components on a metric board is not onerous.

Suitable Grid Settings

For a design such as this simple tutorial circuit, practical grid and design rule settings would be:

Setting	Value	Where
Routing width	0.25 mm	Routing Width design rule
Clearance	0.25 mm	Electrical Clearance design rule
Board definition grid	5 mm	Cartesian Grid Editor
Component placement grid	1 mm	Cartesian Grid Editor
Routing grid	0.25 mm	Cartesian Grid Editor

Setting	Value	Where
Via size	1 mm	Routing Via Style design rule
Via hole	0.6 mm	Routing Via Style design rule

While it might be tempting to select a very fine routing grid so that routing can effectively be placed anywhere, this is not a good approach. Why? because the point of setting the grid to be equal to, or a fraction of, the track+clearance is to ensure that the tracks are placed so that they do not waste potential routing space, which can easily happen if a very fine grid is used.

Select **View » Toggle Units** (or press the **Q** shortcut key) to toggle the workspace units between metric and imperial.

Regardless of the current setting for the units, you can include the units when entering a value in a dialog to force that value to be used, or press the **Ctrl+Q** shortcuts to toggle the units in an open dialog.

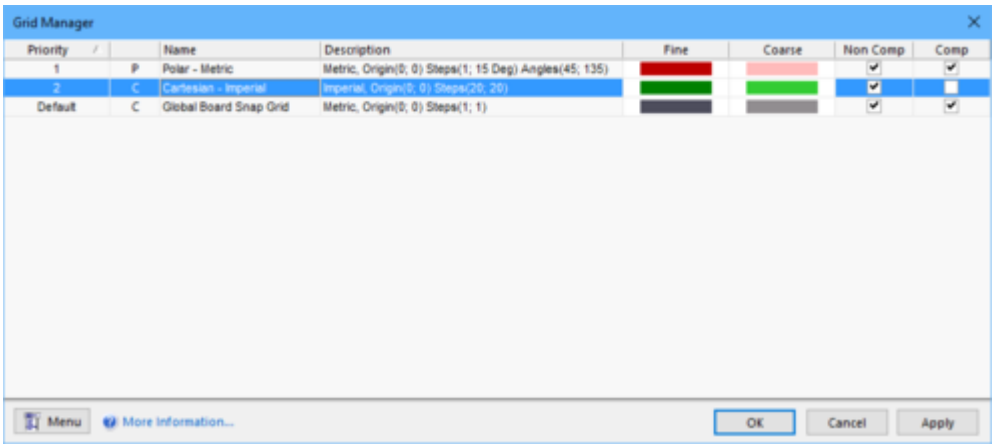
Support for Multiple Grids

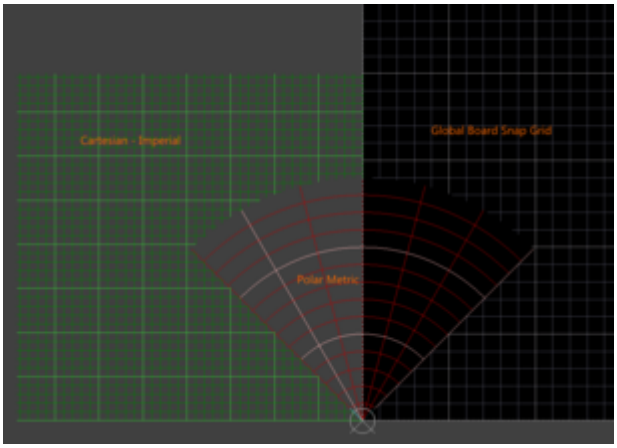
Altium Designer allows multiple snap grids to be defined. There are 2 types of grids supported, **Cartesian** (traditional vertical/horizontal grid) and **Polar** (circular grid).

As well as defining the type of grid, you can also define the area where that grid applies. Note that the Default grid always applies to the entire workspace, even though it is only displayed over the board shape.

Since only one grid can be used at a time, grids also have a priority which is used to determine which grid should be applied when they overlap. There are also controls for defining if a grid is for all objects, components only, or non-components only.

Grids are created and managed in the *Grid Manager*.





Multiple grids can be configured in the *Grid Manager*, an image of these 3 grids is shown on the right (click to enlarge).

The *Grid Manager* is accessed from the **Tools » Grid Manager** command (shortcut: **G, M**). Right-click to add, remove and manage grids, double-click to edit an existing grid.

Only the default grid is used in this tutorial.

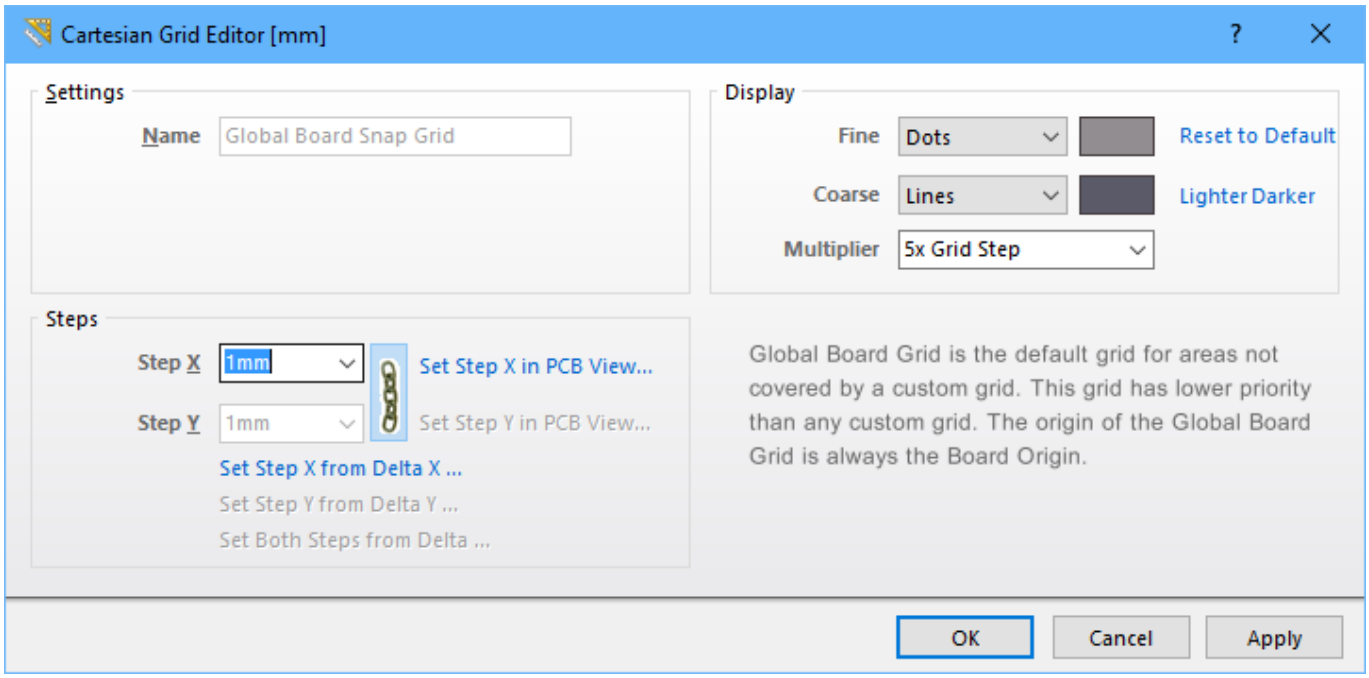
Setting the Snap Grid

Main articles: Grid Manager, Cartesian Grid Editor, Polar Grid Editor

The value of the snap grid you need for the tutorial can be configured via the:

- **right-click » Snap Grid** menu, or the
- *Snap Grid* dialog (**Ctrl+Shift+G**), or the
- *Cartesian Grid Editor* dialog (**Ctrl+G**).

To open the dialog, select **Tools » Grid Manager** to display the *Grid Manager*, then double-click on the **Global Board Snap Grid** to open the *Cartesian Grid Editor*, as shown below.



Set the Snap Grid to 1 mm, ready to position the components.

Configuring the snap grid:

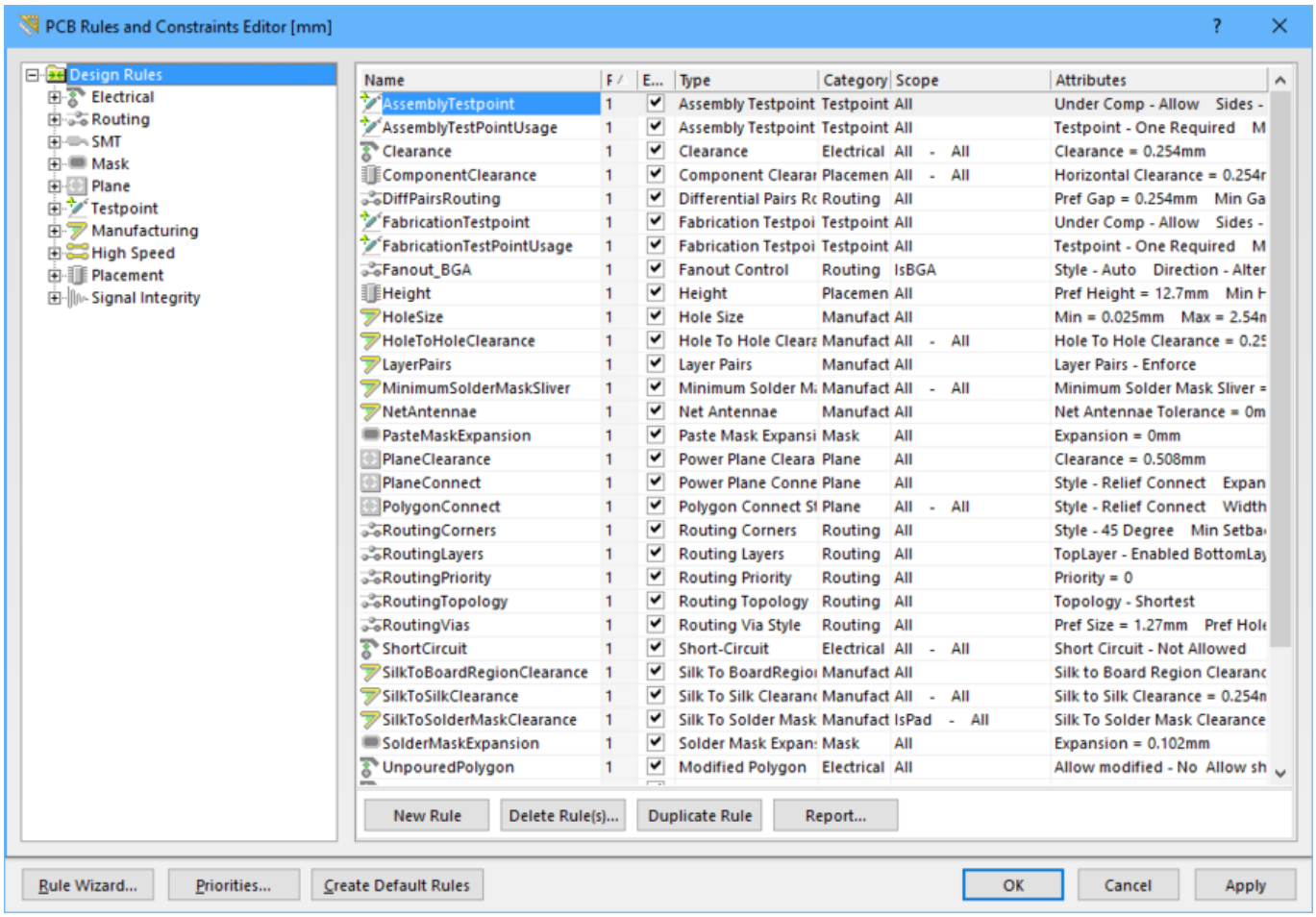
1. Press the **Ctrl+G** shortcut keys to open the *Cartesian Grid Editor* dialog. Alternatively, open the *Cartesian Grid Editor* dialog from the *Grid Manager*, as described above.
2. Type the value `1mm` into the **Step X** field. Because the X and Y fields are linked, there is no need to define the **Step Y** value.
3. To make the grid visible at lower zoom levels set the **Multiplier** to `5x Grid Step`, and to make it easier to distinguish between the two grids, set the **Fine** grid to display as lighter colored `Dots`.
4. Click **OK** to close the dialog.

Setting Up the Design Rules

Main article: PCB Design Rules Reference

The PCB Editor is a rules-driven environment, meaning that as you perform actions that change the design, such as placing tracks, moving components, or autorouting the board, the software monitors each action and checks to see if the design still complies with the design rules. If it does not, then the error is immediately highlighted as a violation. Setting up the design rules before you start working on the board allows you to remain focused on the task of designing, confident in the knowledge that any design errors will immediately be flagged for your attention.

Design rules are configured in the *PCB Rules and Constraints Editor* dialog, as shown below (**Design » Rules**). The rules are divided into 10 categories, which can then be further divided into design rule types.



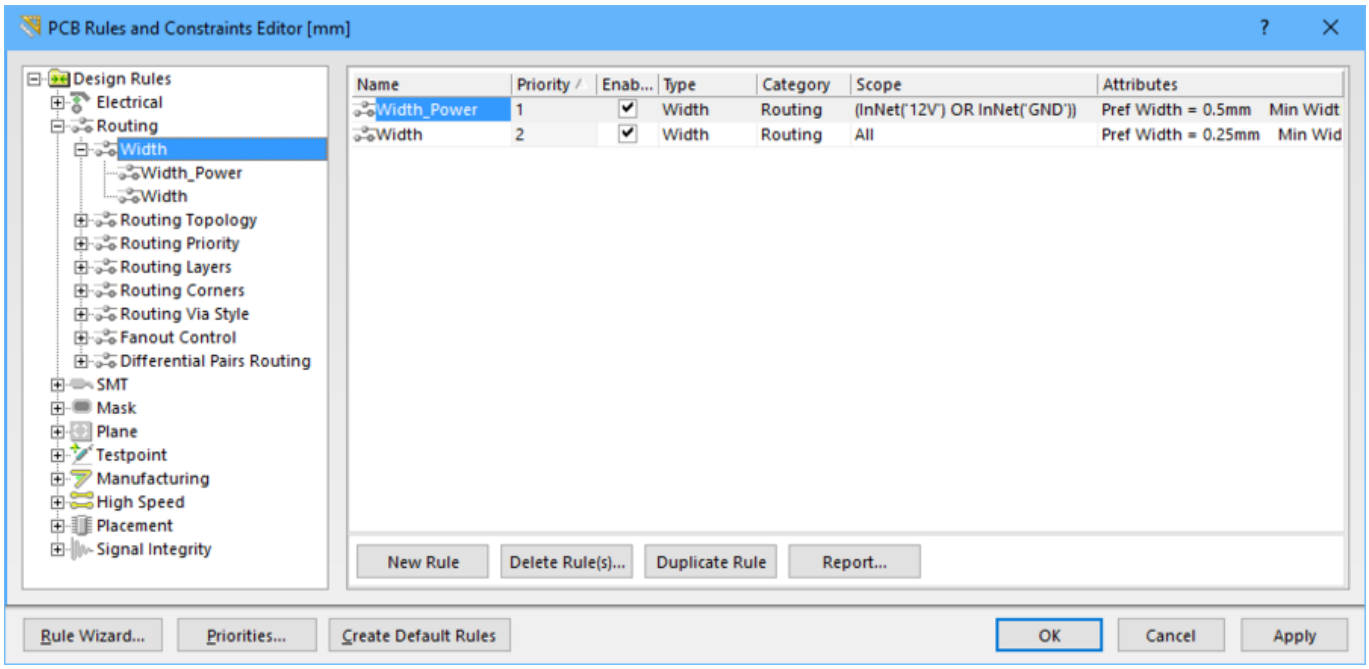
All PCB design requirements are configured as rules/constraints, in the PCB Rules and Constraints Editor.

Routing Width Design Rules

Main article: Width

The width of the routing is controlled by the applicable routing width design rule, which the software automatically selects when you run the **Interactive Routing** command and click on a net. When you are configuring the rules, the basic approach is to set the lowest priority rule to target the largest number of nets, and then add higher-priority rules to target nets with special width requirements, such as power nets. There is no issue if a net is targetted by multiple rules, the software always looks for and only applies the highest priority rule.

For example, the tutorial design includes a number of signal nets, and two power nets. The default routing width rule can be configured at `0.25mm` for the signal nets. This rule will target all nets in the design by setting the rule scope to `All`. Even though a scope of `All` also targets the Power nets, these can be specifically targetted by adding a second, higher-priority rule, with a scope of `InNet('12V') or InNet('GND')`. The image below shows the summary of these two rules, the detail is shown in the images in the following two collapsible sections.



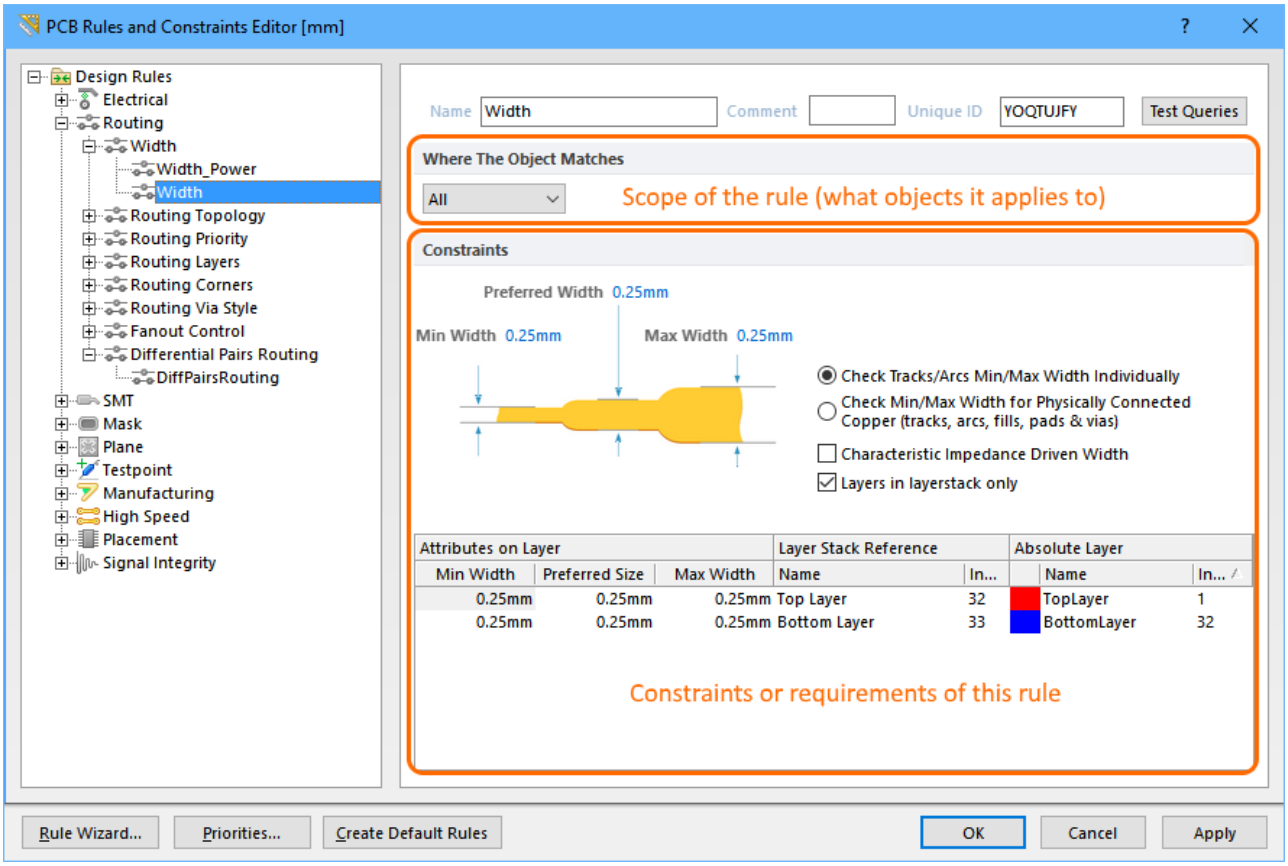
Two Routing Width design rules have been defined, the lowest priority rule targets All nets, the higher priority rule targets objects in the 12V net or the GND net.

Routing Width and Routing Via Style design rules include Min, Max and Preferred settings. Use these if you prefer to have some flexibility during routing, for example when you need to neck a route down, or use a smaller via in a tight area of the board. This can be done on-the-fly as you route, by pressing the **Tab** key to open a dialog and access width/via properties, or by pressing **Shift+W** to select an alternate routing width and **Shift+V** to select an alternate via size. Note that you always remain constrained by the design rules, if you enter a value larger or smaller than permitted by the applicable design rule it will be clipped to the nearest rule value.

Avoid using the Min and Max settings to define a single rule to suit all sizes required in the entire design, doing this means you forgo the ability to get the software to monitor that each design object is appropriately sized for its task.

Configuring the Routing Width Rule for the signal nets:

1. With the PCB as the active document, open the *PCB Rules and Constraints Editor*.
2. Each rules category is displayed under the **Design Rules** folder (left hand side) of the dialog. Double-click on the **Routing** category to expand the category and see the related routing rules. Then double-click on **Width** to display the currently defined width rules.
3. Click once on the existing Width rule to select it. When you click on the rule, the right hand side of the dialog displays the settings for that rule, including: the rule's **Where the First Object Matches** in the top section (also referred to as the rule's *scope* - what you want this rule to target); with the rule's **Constraints** below that.
4. Since this rule is to target the majority of nets in the design (the signal nets), confirm that the **Where the First Object Matches** setting is set to `All`. An additional rule will be added to target the power nets.
5. Edit the **Min Width**, **Preferred Width** & **Max Width** values, setting them to 0.25mm. Note that the settings are reflected in the individual layers shown at the bottom of the dialog, you can also configure the requirements on a per-layer basis.
6. The rule is now defined, click **Apply** to save it and keep the dialog open.



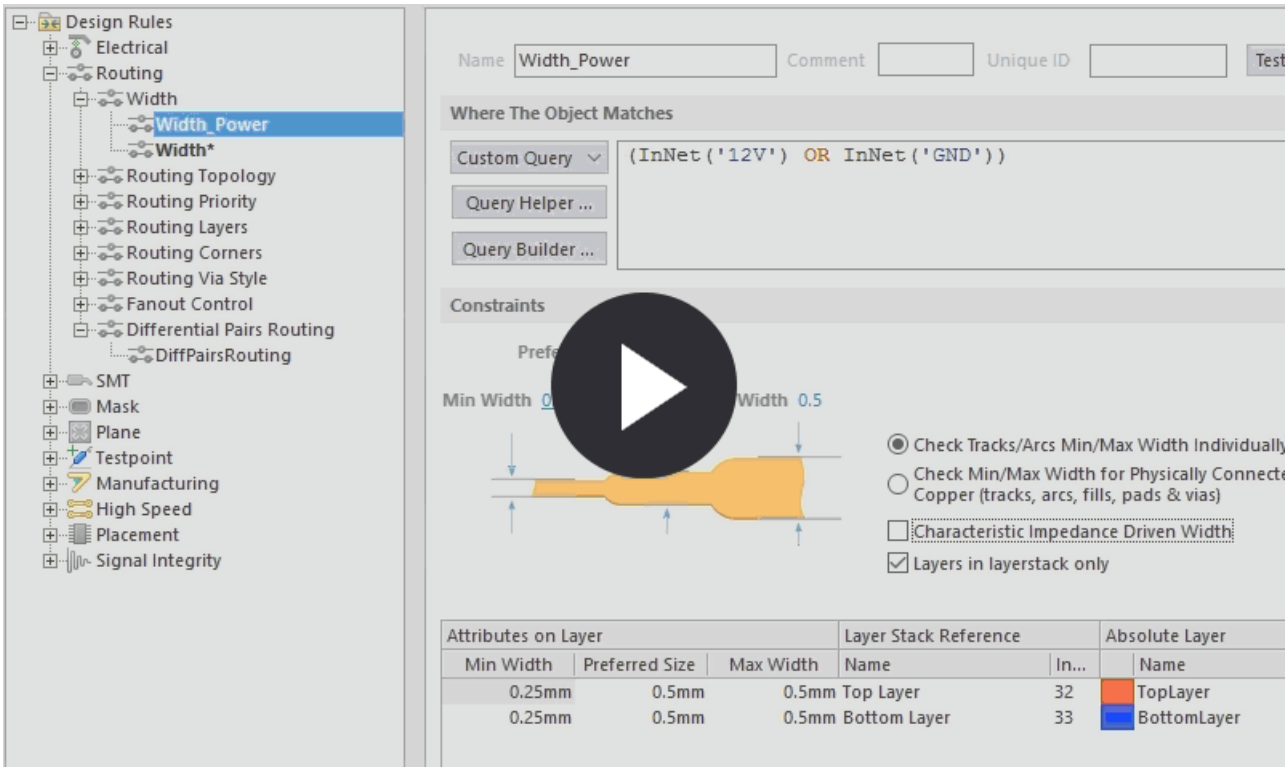
The default Routing Width design rule has been configured.

Adding a Routing Width Rule for the power nets:

1. The next step is to add another design rule to specify the routing width for the power nets. To add and configure this rule, open the *PCB Rules and Constraints Editor*.
2. With the existing Width rule selected in the Design Rules tree on the left of the dialog, right-click and select **New Rule** to add a new Width constraint rule, as shown in the animation below.
3. A new rule named Width_1 appears. Click on the new rule in the Design Rules tree to configure its properties.
4. Click in the **Name** field on the right, and enter the name `Width_Power` in the field.
5. Click the Query Builder button to open the Query Builder, the configure it to target objects:

`InNet('12V') or InNet('GND')`.

6. The last step is to set the Constraints for the rule. Edit the **Min Width** / **Preferred Width** / **Max Width** values `0.25` / `0.5` / `0.5` to allow power net routing widths in the range 0.25mm to 0.5mm, as shown below.



This Width rule targets the power nets.

8. Click **Apply** to save the rules and keep the dialog open.

When there are multiple rules of the same type, the PCB editor uses the rule Priority to ensure the highest prioity applicable rule is applied. When a *new* rule is added it is given the highest priority, and when a rule is *duplicated* the copy is given the priority below the source rule. Click the **Priorities** button down the bottom of the dialog to change priorities.

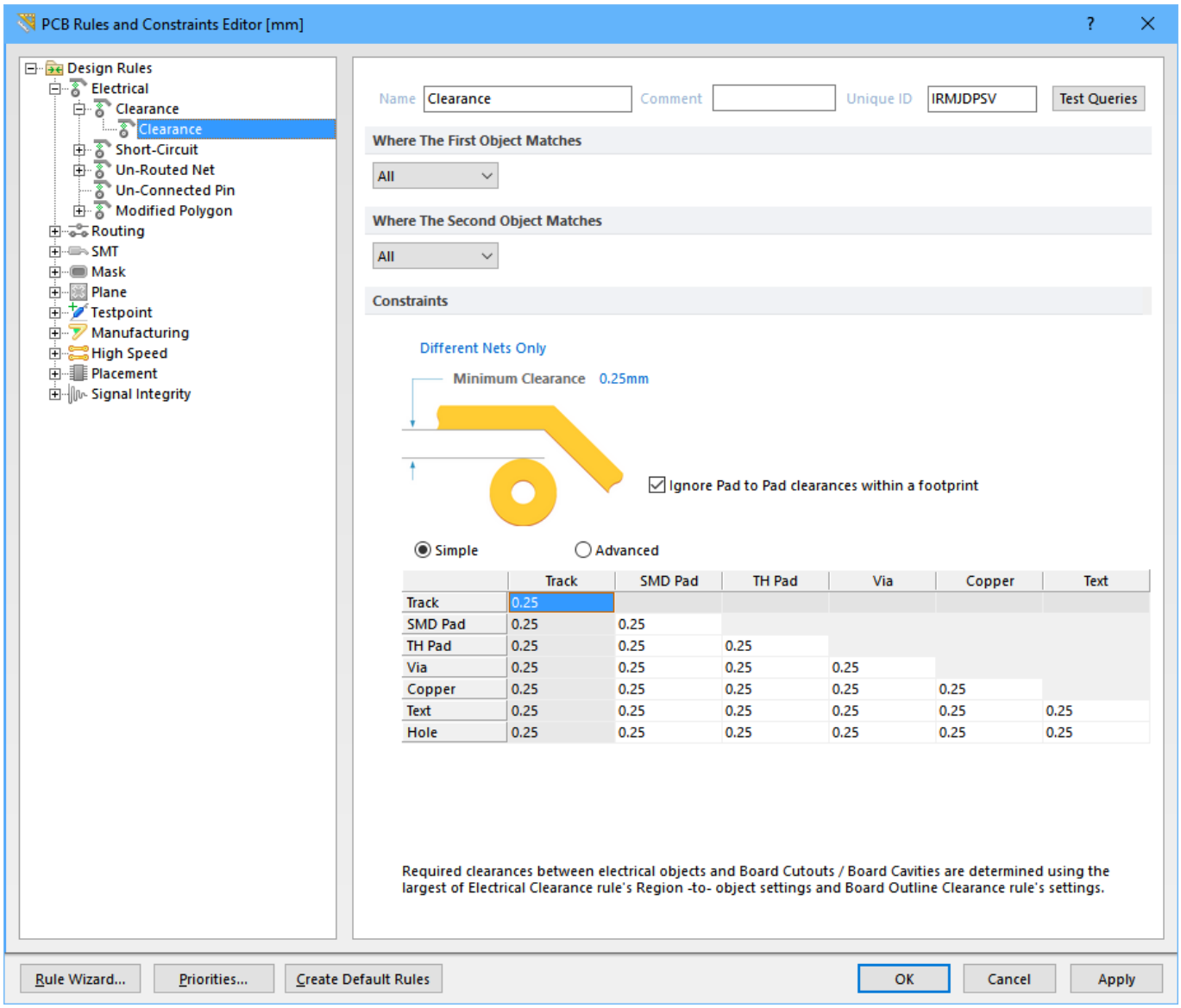
Defining the Electrical Clearance Constraint

Main article: Clearance Constraint

The next step is to define how close electrical objects that belong to different nets, can be to each other.

This requirement is handled by the Electrical Clearance Constraint, for the tutorial a clearance of `0.25mm` between all objects is suitable.

Note that entering a value into the **Minimum Clearance** field will automatically apply that value to all of the fields in the grid region at the bottom of the dialog. You only need to edit in the grid region when you need to define a clearance based on the object-type.



The electrical clearance constraint is defined between objects. Switch the Constraints to Advanced to display all object kinds.

Note that the Electrical Clearance Constraint has two object selection fields, **Where the First Object Matches** and **Where the Second Object Matches**. That is because this is a binary rule - it is a rule that applies *between* 2 objects.

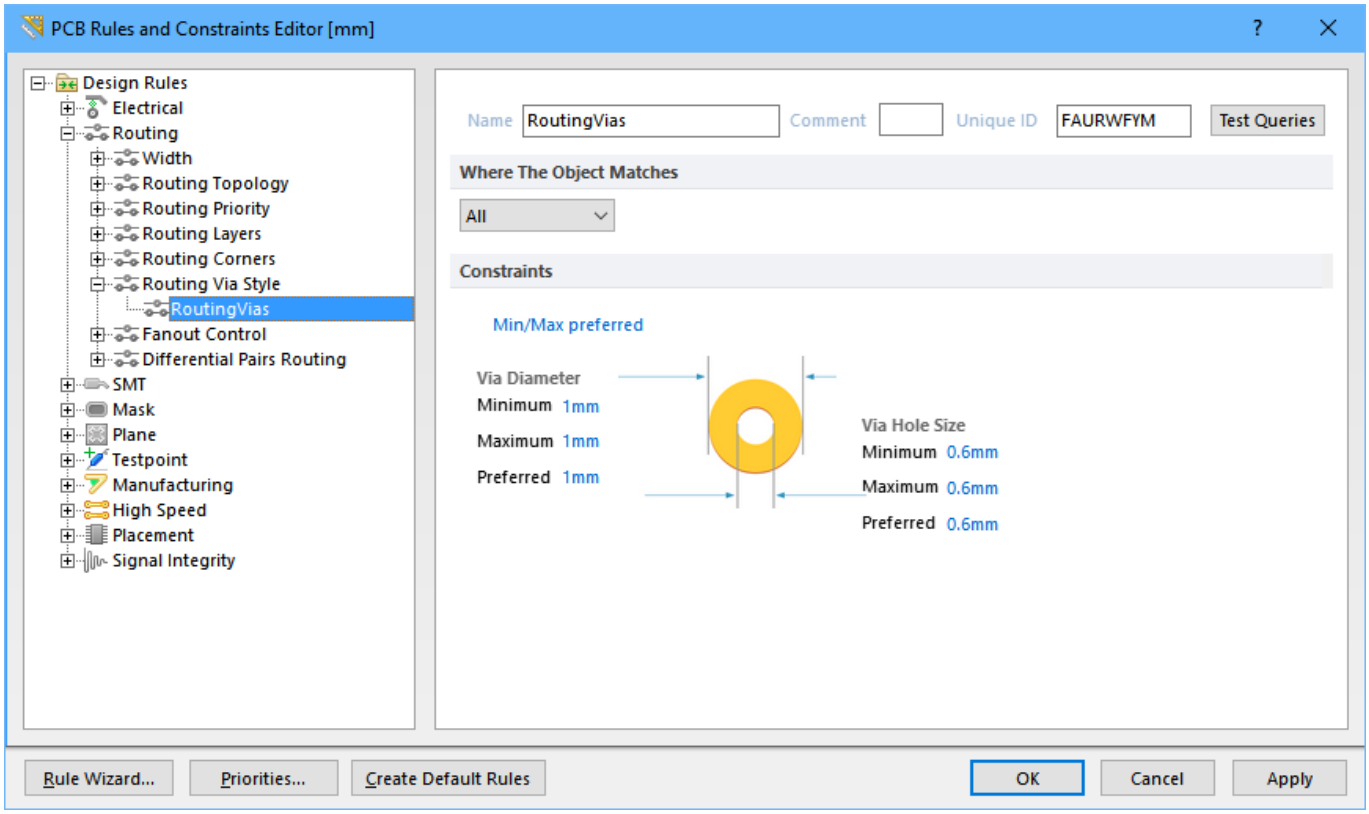
Defining the Electrical Clearance Constraint:

1. Expand the Electrical category in the tree of Design Rules, then expand the Clearance rule-type.
2. Click to select the existing Clearance constraint. Note that this rule has two **Full Query** fields, that is because it is a *Binary rule*. The rules engine checks each object targeted by the setting **Where the First Object Matches** and checks it against the objects targeted by the **Where the Second Object Matches** setting, to confirm that they satisfy the specified **Constraints** settings. For this design, this rule will be configured to define a single clearance between `All` objects.
3. In the **Constraints** region of the dialog, set the **Minimum Clearance** to `0.25mm`, as shown in the image above.
4. Click **Apply** to save the rule and keep the dialog open.

Defining the Routing Via Style

Main article: Routing Via Style

As you route and change layers a via is automatically added, in this situation the via properties are defined by the applicable Routing Via Style design rule. If you place a via from the Place menu, its values are defined by the in-built default primitive settings. For the tutorial, you will configure the Routing Via Style design rule.



A single routing via is suitable for all nets in this design.

Defining the Routing Via Style Design Rule:

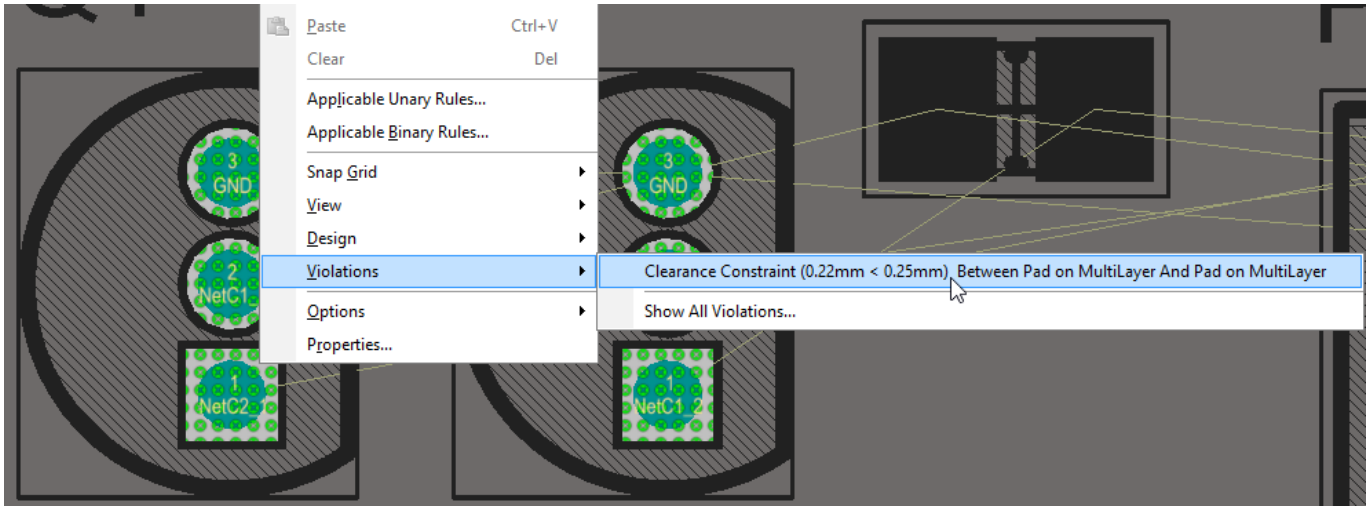
1. Expand the Design Rule tree and select the default RoutingVias design rule.
2. Since it is highly likely that the power nets can be routed on a single side of the board, it is not necessary to define a routing via style rule for signal nets and another routing via style rule for power nets. Edit the rule settings to the values suggested earlier in the tutorial, that is a **Via Diameter** = `1mm` and a **Via Hole Size** = `0.6mm`. Set all fields (Min, Max, Preferred) to the same size.
3. Click **OK** to close the *PCB Rules and Constraints Editor*.

4. Save the PCB file.

Existing Design Rule Violation

You might have noticed that the transistor pads are showing that there is a violation. Right-click over a violation and select the **Violations** in the right-click menu, as shown below. The details show that there is a:

- Clearance Constraint violation
- Between a Pad on the MultiLayer, and a Pad on the MultiLayer
- Where the clearance is 0.22mm, which is less than the specified 0.25mm



Right-click on a violation to examine what rule is being violated, and the violation conditions. In this image the display is in single layer mode, with the multi-layer as the active layer.

> This violation will be discussed and resolved shortly. If you find the violation markers distracting, you can clear them by running the **Tools » Reset Error Markers** command. This command only clears the marker, it does not hide or remove the actual error. The error will be flagged again the next time you perform an edit action that runs the online DRC (such as moving the component), or when you run the batch DRC.

Altium Designer's internal defaults for a new board are Imperial. That means when you switch to Metric, settings such as the Soldermask expansion will change from rounded values like 4mil, to 0.102mm, or the Minimum Solder Mask Sliver default will change from 10mil to 0.254mm. While that least significant digit, such as 0.002mm, is insignificant when it comes to output generation, you can edit these settings in the design rules if it bothers you. Select **Design Rules** at the top of the tree on the left of the *PCB Rules and Constraints Editor*, then you can scan down the **Attributes** column for all of the rules and quickly locate any that need their values adjusted.

Design rules can also be exported and stored in a `.RUL` file, and then imported into future PCB designs. To do this, right-click in the tree on the left of the *PCB Rules and Constraint Editor* to open the *Choose Design Rules* dialog. Select the rules you wish to export using the standard Windows selection techniques, then click **OK** to export the selected rules.

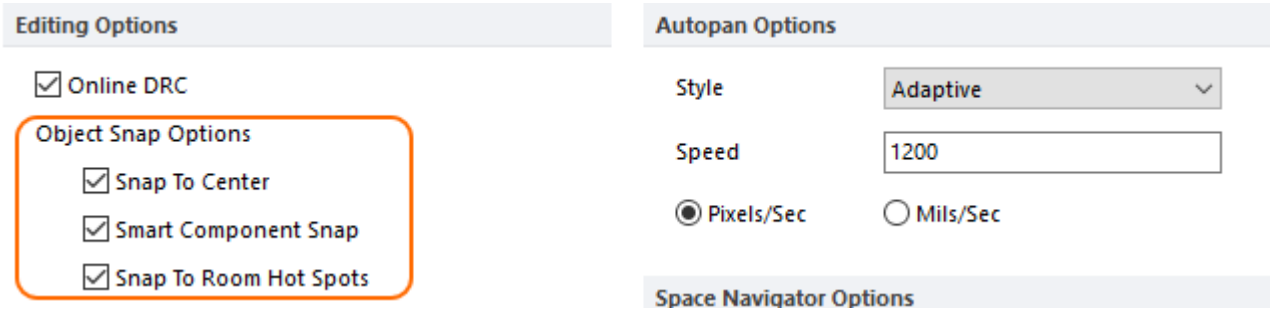
Positioning the Components on the PCB

There is a saying that PCB design is 90% placement and 10% routing. While you could argue about the percentage of each, it is generally accepted that good component placement is critical for good board design. Keep in mind that you may need to tune the placement as you route too.

Component Positioning and Placement options

When you click and hold on a component to move it, if the **Snap to Center** option is on, then the component will move to be held by its reference point. The reference point is the 0,0 coordinate of the component, when it was built in the library editor.

The **Smart Component Snap** option allows you to override this snap to center behavior and snap to the nearest component pad instead, handy when you need to position a specific pad in a specific location.



Enable Snap to Center to always hold the component by its reference point. Smart Component Snap is helpful when you need to align by a specific pad.

Setting the component positioning options:

1. Select **DXP » Preferences** to open the *Preferences* dialog.
2. Open the **PCB Editor - General** page of the dialog, in the **Editing Options** section, make sure the **Snap To Center** option is enabled. This ensures that when you "grab" a component to position it, the cursor will hold the component by its reference point.
3. Note the **Smart Component Snap** option, if this is enabled you can force the software to snap to a pad center instead of the reference point by clicking and holding closer to the required pad than the component's reference point. This is very handy if you require a specific pad, to be on

a specific grid point. It can work against you if you are working with small surface mount components though, as it can make it harder to "grab" them by their reference point.

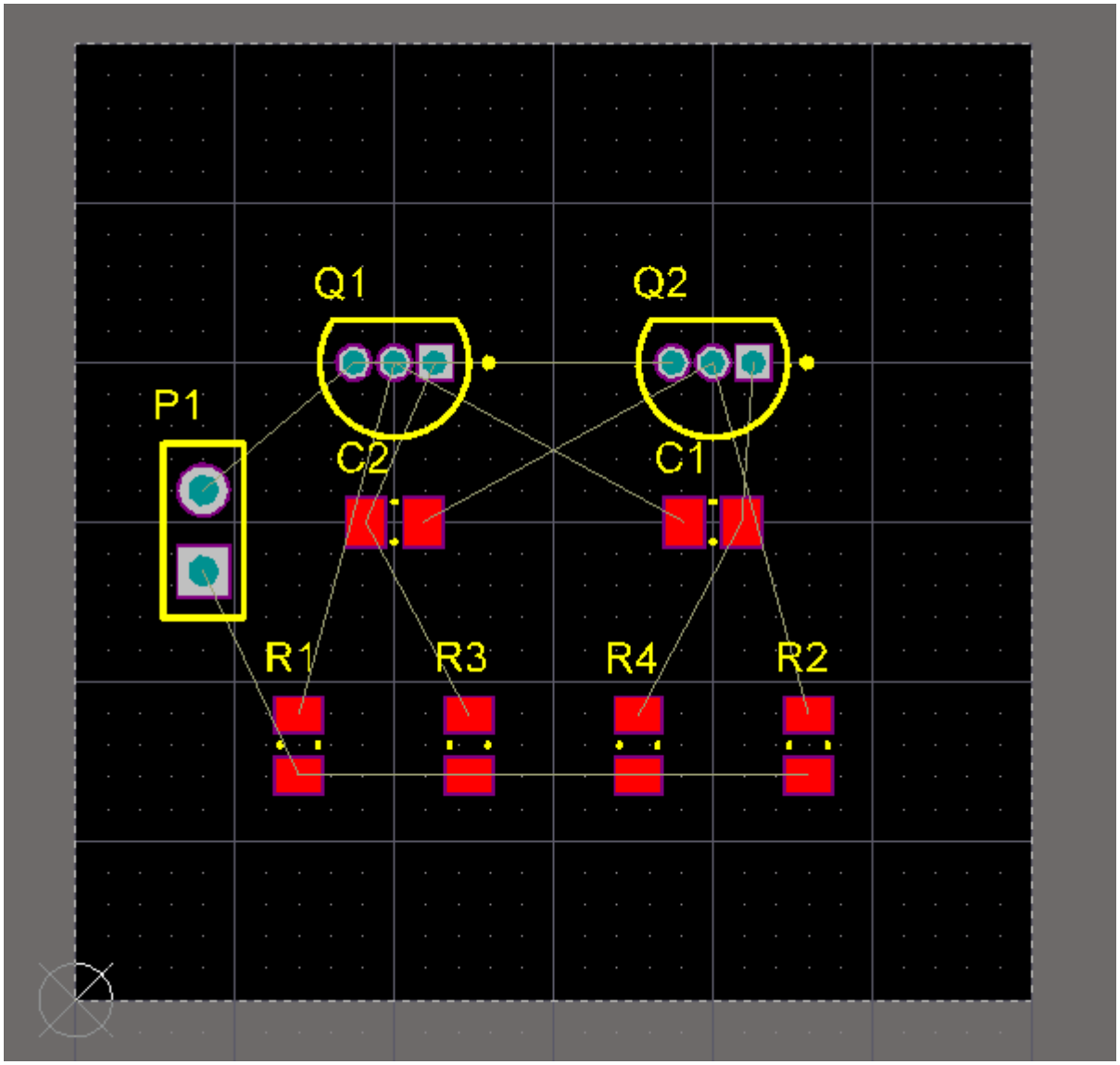
Positioning Components

You can now position the components in suitable locations on the board.

To move a component, either:

- **Click-and-Hold** the left mouse button on the component, move it to the required location, rotate it with the **Spacebar**, then release the mouse button to place it; or
- Run the **Edit » Move » Component** command, then single click to pick up a component, move it to the required location, rotate if required, then click once to place it. When you are finished, right-click to drop out of the **Move Component** command.

The connection lines are automatically re-optimized as you move a component - use them to help orient and position the components so that there is the least amount of connection line cross-overs.



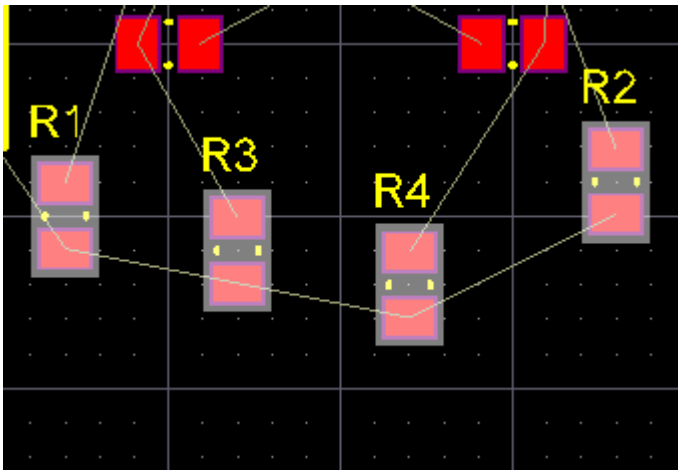
Components positioned on the board.

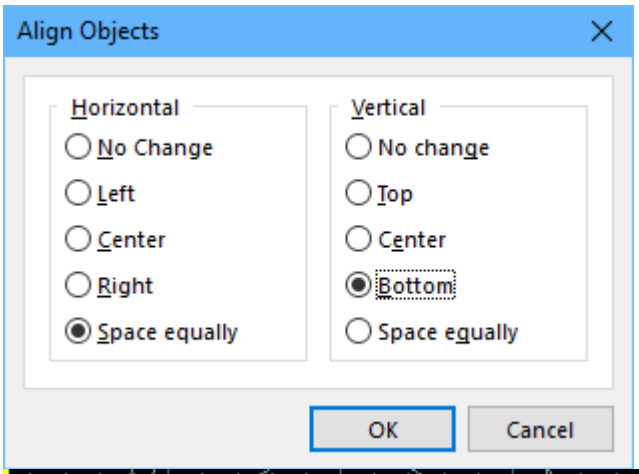
[Positioning the components:]

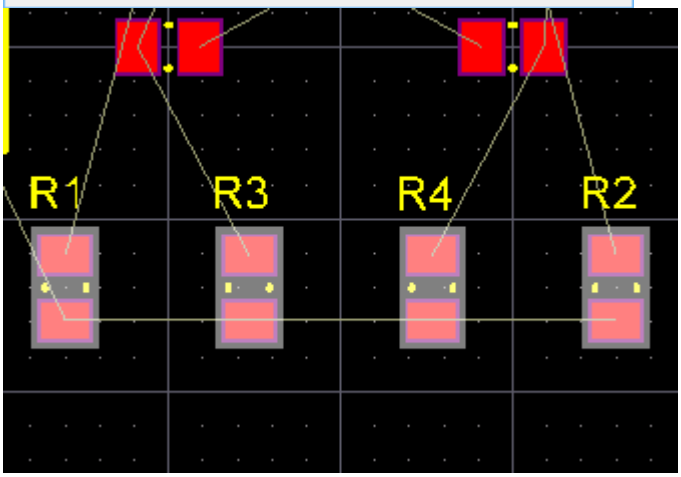
1. Zoom to display the board and the component. One way to do this is to zoom out (**PgDn**) so the board and the components are all visible, then **right-click** and choose **View » View Area**, then click to define the top left and bottom right of the exact area you wish to view.
2. The components will be positioned on the current Snap grid. For a simple design such as this there are no specific design requirements that dictate what placement grid should be used, as the designer, you decide what a suitable placement grid would be. To simplify the process of positioning the components you can work with a coarse placement grid, for example 1mm. Check the Status bar to confirm that the **Snap Grid** is set to 1mm, press **Ctrl+Shift+G** to change the grid if required.
3. The components in the tutorial can be placed as shown in the image above. To place connector P1, position the cursor over the middle of the outline of the connector, and **Click-and-Hold** the left mouse button. The cursor will change to a cross hair and jump to the reference point for the part. While continuing to hold down the mouse button, move the mouse to drag the component.
4. Press the **Spacebar** to rotate the component if required, and position the footprint towards the left-hand side of the board, as shown in the figure above.
5. When the connector component is in position, release the mouse button to drop it into place. Note how the connection lines drag with the component.
6. Reposition the remaining components, using the figure above as a guide. Use the **Spacebar** to

rotate (increments of 90º anti-clockwise) components as you drag them, so that the connection lines are as shown in the figure.

7. Component text can be repositioned in a similar fashion - click-and-drag the text and press the **Spacebar** to rotate it.
8. The PCB editor also includes powerful interactive placement tools. Let's use these to ensure that the four resistors are correctly aligned and spaced.
9. Holding the **Shift** key, click on each of the four resistors to select them, or click and drag the selection box around all 4 of them. A shaded selection box will display around each of the selected components, in the color set for the system color called **Selections**.
10. Right-click on any of the selected components and choose **Align » Align** to open the *Align Objects* dialog.
11. Select **Space Equally** in the **Horizontal** section and **Bottom** in the **Vertical** section, then click **OK** to apply these changes. The four resistors are now aligned (with the lowest component) and equally spaced.







Select, then align and space the resistors.

12. Click elsewhere in the design window to de-select all the resistors. If required you can also align the capacitors and transistors, although this might not be required since you have a coarse Snap grid at the moment.
13. Save the PCB file.

Selected objects can also be moved using the keyboard rather than the mouse. To do this, hold **Ctrl**, then each time you press an **Arrow** key the selection will move 1 grid step in the direction of that arrow. Include the **Shift** key to move selected objects in 10x Snap Grid steps.

When you are moving a component with the mouse, you can constrain it to an axis by holding the **Alt** key. The component will attempt to hold the same horizontal axis (if moving horizontally) or vertical axis (if moving vertically) - move it further from the axis to override this behavior, or release the **Alt** key.

With everything positioned, it's time to do some routing!

Interactively Routing the Board

Main article: Interactive Routing

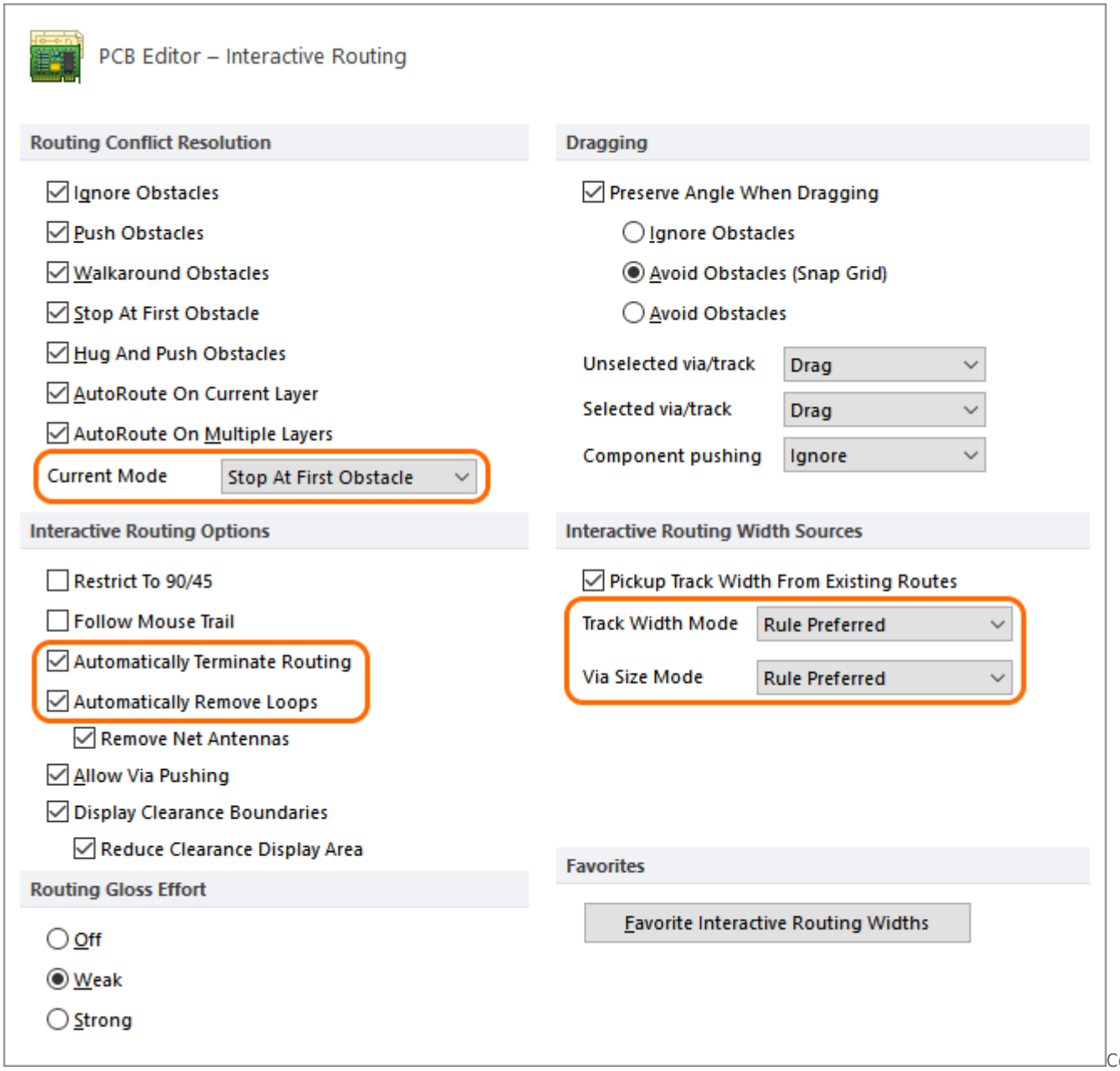
Routing is the process of laying tracks and vias on the board to connect the component pins. The PCB editor makes this job easy by providing sophisticated interactive routing tools, as well as the topological autorouter, which optimally routes the whole or part of a board at the click of a button. While autorouting provides an easy and powerful way to route a board, there will be situations where you will need exact control over the placement of tracks. In these situations you can manually route part or all of your board.

In this section of the tutorial, you will manually route the entire board single-sided, with all tracks on the top layer. The Interactive Routing tools help maximize routing efficiency and flexibility in an intuitive way, including cursor guidance for track placement, single-click routing of the connection, pushing obstacles, automatically following existing connections, all in accordance with applicable design rules.

Preparing for Interactive Routing

Main article: PCB Editor - Interactive Routing

Before starting to route, it is important to configure the Interactive Routing options found in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.



Configure the interactive routing options.

[Preparing for interactive routing:]

1. Set the **Routing Conflict Resolution Current Mode** to `Stop at First Obstacle`. You can cycle through the enabled modes interactively as you route by pressing **Shift+R**.
2. In the **Interactive Routing Options** section of the page, confirm that the **Automatically Terminate Routing** and the **Automatically Remove Loops** options are enabled. The first option releases the cursor from the current route when you click on a pad to finish that route. The second option allows you to change existing routing by simply routing an alternate path - you route a new path until it meets the old path (creating a loop), then right-click to indicate it is complete - the software then automatically removes the old, redundant part of the routing. This feature will be explored later in the tutorial.
3. Confirm that the **Interactive Routing Width / Via Size Sources** options are both set to **Rule Preferred**.
4. Press **Ctrl+Shift+G** to open the *Snap Grid* dialog and set the Snap Grid to `0.25mm`.

Time to set the Snap Grid to a value that is suitable for routing. Press **Ctrl+Shift+G** to open

the *Snap Grid* dialog and set the Snap Grid to `0.25mm`.

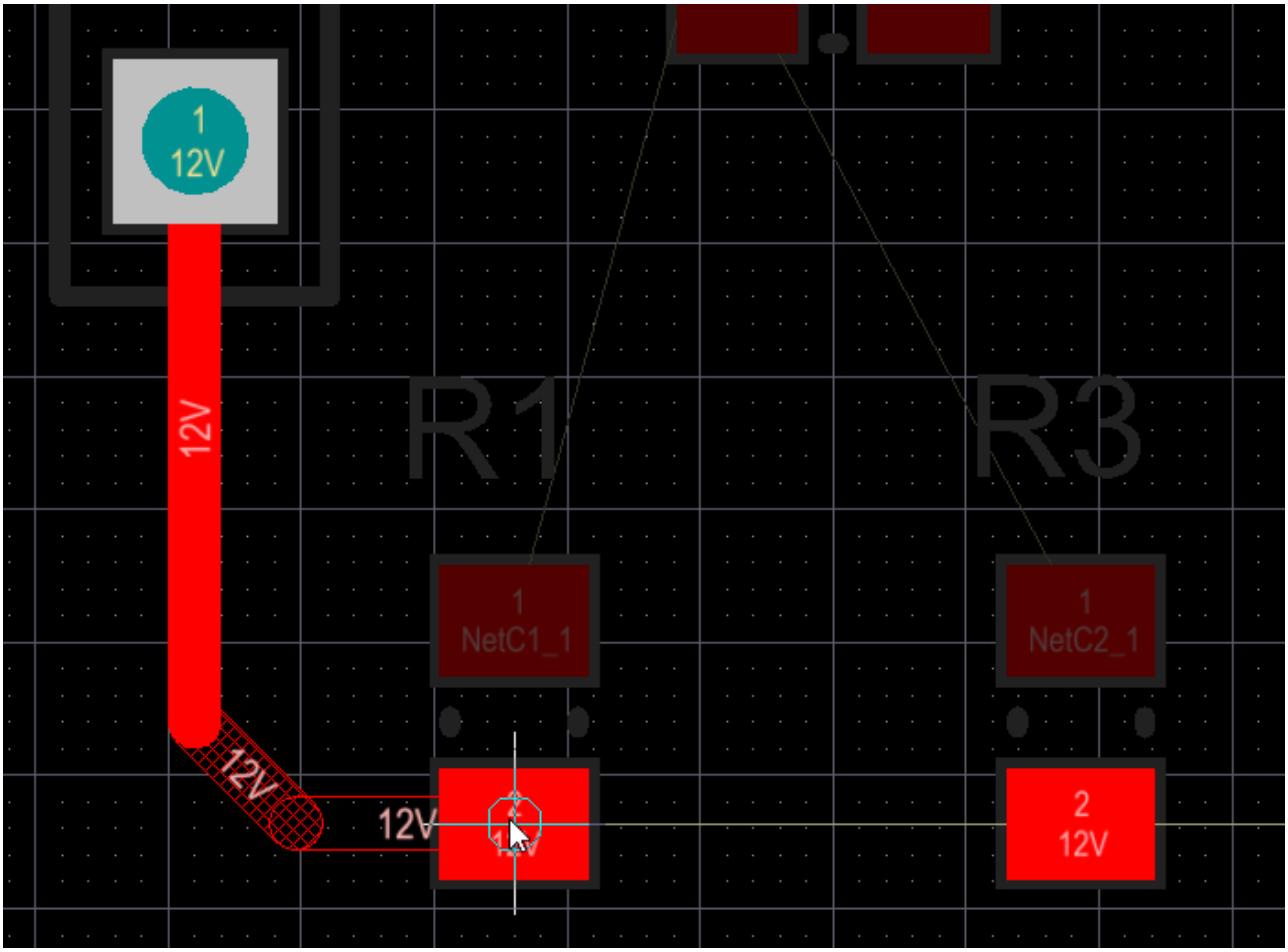
Time to Route

- Interactive routing is launched by clicking the Route button , or selecting the routing command, **Route » Interactive Routing** (shortcut: **U, T** or **P, T)**).
- Since the components are mostly surface mount and the design is simple, the board can be routed on the top layer. As you place tracks on the top layer of the board, you use the ratsnest (connection lines) to guide you.
- Tracks on a PCB are made from a series of straight segments. Each time there is a change of direction, a new track segment begins. Also, by default the PCB editor constrains tracks to a vertical, horizontal or 45° orientation, allowing you to easily produce professional results. This behavior can be customized to suit your needs, but for this tutorial you can use the defaults.
- After reaching the target pad, **right-click** or press **Esc** to release that connection - you will remain in Interactive Routing mode, ready to click on the next connection line.

A simple animation showing the board being routed. Note that many of the connections are finished using the Ctrl+Click to autocomplete feature.

Interactively routing the board:

1. Check which layers are currently visible by looking at the Layer Tabs at the bottom of the workspace. If the Bottom Layer is not visible, press the **L** shortcut to open the *View Configurations* dialog, and enable the **Bottom Layer**.
2. Click on the **Top layer** tab at the bottom of the workspace to make it the current, or active layer, ready to route on.
3. It is often easier to route in single layer mode, press **Shift+S** to toggle to in and out of single layer mode.
4. Click button on the Wiring Toolbar, select **Interactive Routing** from the **Place** menu, or right-click and choose **Interactive Routing** from the context menu. The cursor will change to a crosshair, indicating you are in interactive routing mode.
5. Position the cursor over the lower pad on connector P1. As you move the cursor close to the pad it will automatically snap to the center of the pad - this is the **Snap To Object Hotspot** feature *pulling* the cursor to the center of the nearest electrical object (configure the **Range** of attraction in the **Board Options** dialog). Sometimes the **Snap To Object Hotspot** feature pulls the cursor when you don't want it to, in this situation press the **Ctrl** key to temporarily inhibit this feature.
6. **Left-Click** or press **Enter** to anchor the first point of the track.
7. Move the cursor towards the bottom pad of the resistor R1, and click to place a vertical segment. Note how track segments are displayed in different ways (as shown in the image below). During routing, the segments are shown as:
    - **Solid** - the segment has been placed.
    - **Hatched** - hatched segments are proposed but uncommitted, they will be placed when you left-click.
    - **Hollow** - this is referred to as the look-ahead segment, it allows you to work out where the last proposed segment should end. This segment is *not* placed when you click, unless the next click will complete the route. In this situation the **Automatically Terminate Routing** option kicks in and overrides the default look-ahead behavior. The look-ahead mode can be toggled on/off using the **1** shortcut during routing.



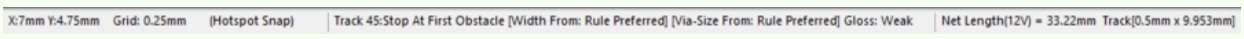
Note how the segments are displayed differently.

8. Manually route by **Left-Clicking** to commit track segments, finishing on the lower pad of R1. Note how each mouse click places the hatched segment(s). For the connection that you are currently routing, press **Backspace** to rip up the last-placed segment.
9. Rather than routing all the way to the target pad, you can also press **Ctrl+Left Click** to use the *Auto-Complete* function and immediately route the entire connection. Auto-complete behaves in the following way:
    - It takes the shortest path, which may not the best path as you need to always consider paths for other connections yet to be routed. If you are in Push mode (shown on the Status bar when routing), Auto-complete can push existing routes to reach the target.
    - On longer connections, the Auto-Complete path may not always be available as the routing path is mapped section by section, and complete mapping between source and target pads may not be possible.
    - You can also Auto-complete directly on a pad or connection line.
10. Continue to route all the connections on the board.
11. Use the techniques detailed above to route all of the connections between the other components on the board. The simple animation above shows the board being interactively routed.
12. There is no single solution to routing a board, so it is inevitable that you will want to change the routing. The PCB editor includes features and tools to help with this, they are discussed in the following sections and are also demonstrated in the animation shown above.
13. Save the design when you are finished routing.

Routing Tips

Keep in mind the following points as you are routing:

Keystroke	Behavior
~ (tilda) or **Shift+F1**	Pop up a menu of interactive shortcuts - most settings can be changed on the fly by pressing the appropriate shortcut, or selecting from the menu.
* or **Ctrl+Shift+WheelRoll**	Switch to the next available signal layer. A via is automatically added, in accordance with the applicable Routing Via Style design rule.
Shift+R	Cycle through the enabled conflict resolution modes. Enable the required modes in the **Interactive Routing** preferences page.
Shift+S	Toggle single layer mode on and off - ideal when there are many objects on multiple layers.
Spacebar	Toggle the current corner direction.
Shift+Spacebar	Cycle through the various track corner modes. The styles are: any angle, 45°, 45° with arc, 90° and 90° with arc. There is an option to limit this to 45° and 90° in the **Interactive Routing** preferences page.
Ctrl+Left-Click	Auto-complete the connection being routed. Auto-complete will not succeed if there are unresolvable conflicts with obstacles.
Ctrl	Temporarily suspend the Hotspot Snap, or press **Shift + E** to cycle through the 3 available modes (off / on for current layer / on for all layers).
End	Redraw the screen.
PgUp / PgDn	Zoom in / out, centered around the current cursor position. Alternatively, use the standard Windows mouse wheel zoom and pan shortcuts.
Backspace	Remove the last-committed track segment.
Right-click or **ESC**	Drop the current connection, remaining in Interactive Routing mode.



Keep an eye on the **Status bar**, it displays important information during interactive routing, including:

- Current workspace location and Snap Grid setting
- Hotspot Snap: off / on for current layer / on for all layers
- Current track corner mode
- Current Interactive Routing Mode
- Source of routing Width
- Source of routing Via Style
- Current Gloss strength
- Name of Net
- Overall route length
- Dimensions of routing segment being placed

Interactive Routing Modes

The PCB editor's Interactive Routing engine supports a number of different modes, with each mode helping the designer deal with particular situations. Press the **Shift+R** shortcut to cycle through these modes as you interactively route, note that the current mode is displayed on the Status bar.

The available interactive routing modes include:

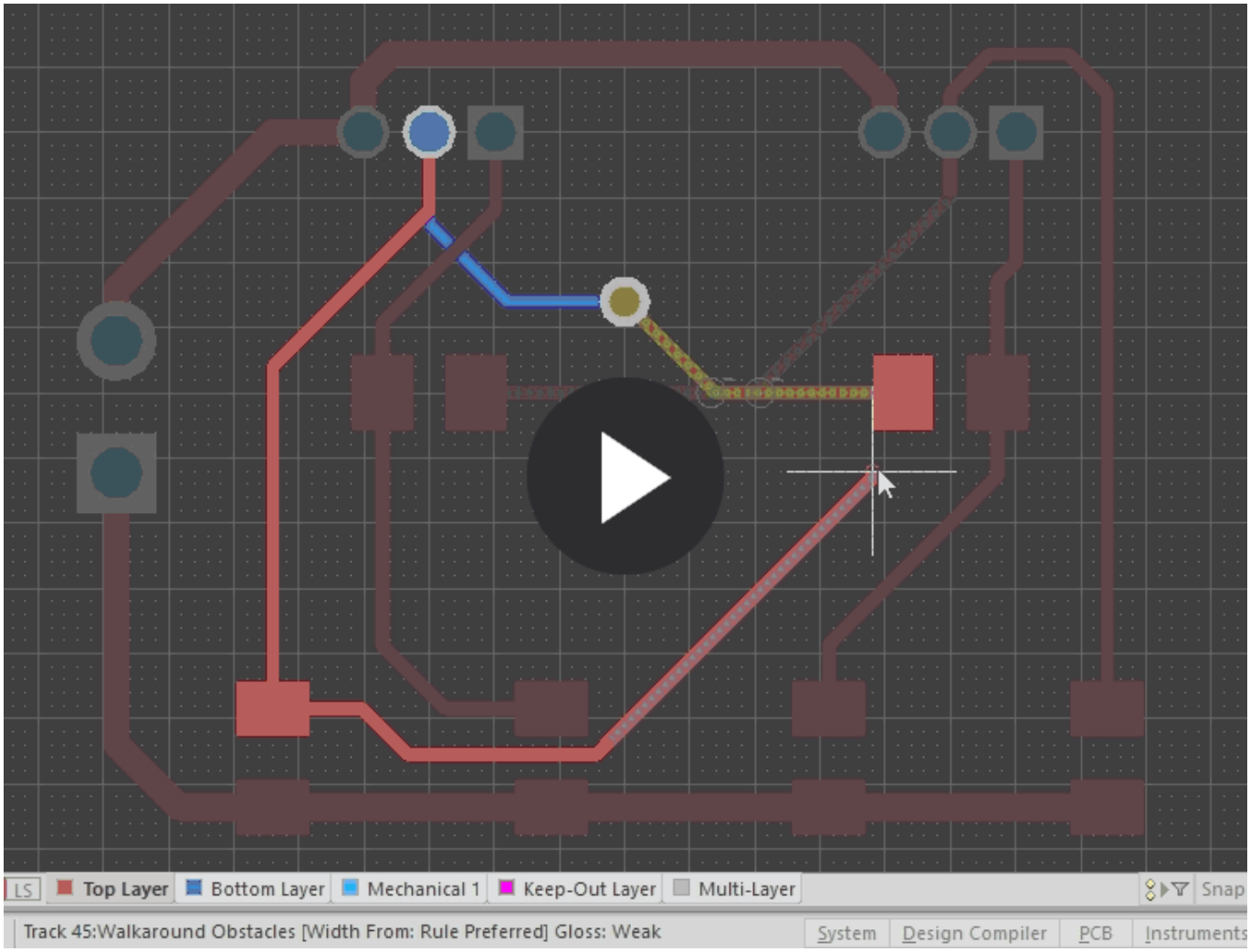
- **Ignore Obstacles** - This mode lets you place tracks anywhere, including over existing objects, displaying but allowing potential violations.
- **Push Obstacles** - This mode will attempt to move objects (tracks and vias), which are capable of being repositioned without violation, to accommodate the new routing.
- **Walkaround Obstacles** - This mode will attempt to find a routing path around existing obstacles without attempting to move them.
- **Stop at first Obstacle** - In this mode the routing is essentially manual, as soon as an obstacle is encountered the track segment will be clipped to avoid a violation.
- **Hug & Push Obstacles** - This mode is a combination of Walkaround and Push. It will hug as it performs a Walkaround of obstacles, however, will also attempt to Push against fixed obstacles when there is insufficient clearance to continue using Walkaround.
- **Autoroute on Current Layer** - this mode brings basic autorouting functionality to interactive routing, it can automatically select between walkaround and push, based on heuristics that consider push distance, versus walk distance and route length. Like an autorouter, this mode can deliver better results on a complex, busy board, than on a simple, unrouted board.
- **Autoroute on Multiple Layers** - this mode also brings basic autorouting functionality to interactive routing, it can also automatically select between walkaround and push, based on heuristics that consider push distance, versus walk distance and route length. This mode can also place a via and consider using other routing layers. Like an autorouter, this mode can deliver better results on a complex, busy board, than on a simple, unrouted board.

Modifying and Rerouting

To modify an existing route, there are two approaches, either: *reroute*, or *re-arrange*.

Reroute an existing Route

- There is no need to un-route a connection to redefine its path, simply click the Route button  and start routing the new path.
- The Loop Removal feature will automatically remove any redundant track segments (and vias) as soon as you close the loop and right-click to indicate you are complete (the Loop Removal feature was enabled earlier in the tutorial).
- You can start and end the new route path at any point, swapping layers as required.
- You can also create temporary violations by switching to Ignore Obstacle mode (as shown in the animation below), which you later resolve.

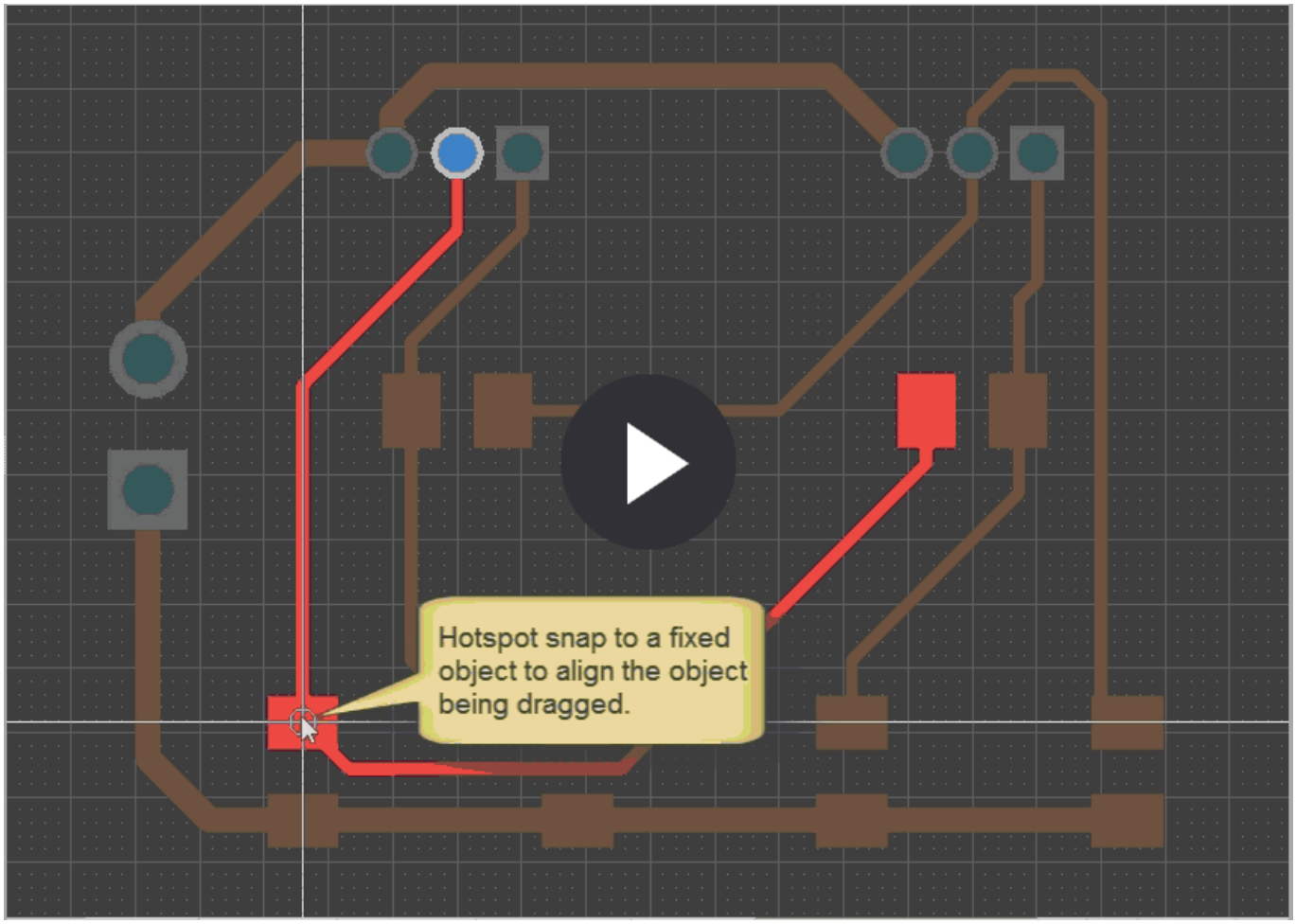


A simple animation showing the Loop Removal feature being used to modify existing routing.

Loop Removal is enabled in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog. Note that there are situations where you may want to create loops, for example power net routing. If necessary, Loop Removal can be disabled for an individual net by editing that net in the *PCB* panel. To access the option set the panel to **Nets** mode, then double click on the net name in the panel to open the *Edit Net* dialog.

Re-arrange Existing Routes

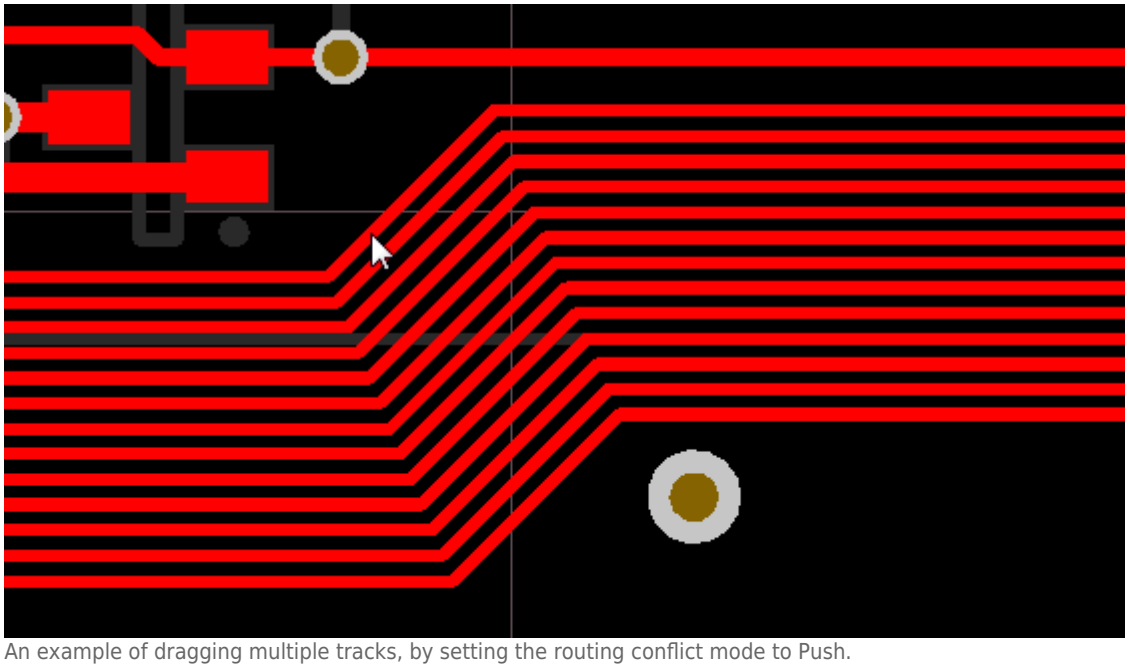
- To interactively slide or drag track segments across the board, simply click, hold and drag, as shown in the animation below. The default dragging behavior is configured in the **PCB - Interactive Routing** page of the *Preferences* dialog, as shown in the animation below.
- The PCB editor will automatically maintain the 45/90 degree angles with connected segments, shortening and lengthening them as required.



An animation showing track dragging being used to tidy up existing routing.

Track Dragging Tips

- Change the default select-then-drag mode using the **Unselected via/track** and **Selected via/track** options in the **PCB Editor - Interactive Routing** page of the *Preferences* dialog.
- During dragging the routing conflict resolution modes also apply (Ignore, Push, HugNPush), press **Shift+R** to cycle through the modes as you drag a track segment.
- Existing pads and vias will be jumped, or vias will be pushed if necessary and possible, if Push mode is enabled.
- To convert a 90 degree corner to a 45 degree route, start dragging on the corner vertex.
- While dragging you can move the cursor and hotspot snap it to an existing, non-moving object such as a pad (shown above) - use this to help align the new segment location with an existing object and avoid very small segments being added.
- To break a single segment, select the segment first, then position the cursor over the center vertex to add in new segments.



An example of dragging multiple tracks, by setting the routing conflict mode to Push.

Automatically Routing the Board

Before you begin exploring the autorouter, save your board so you can return to the interactively routed version if you want.

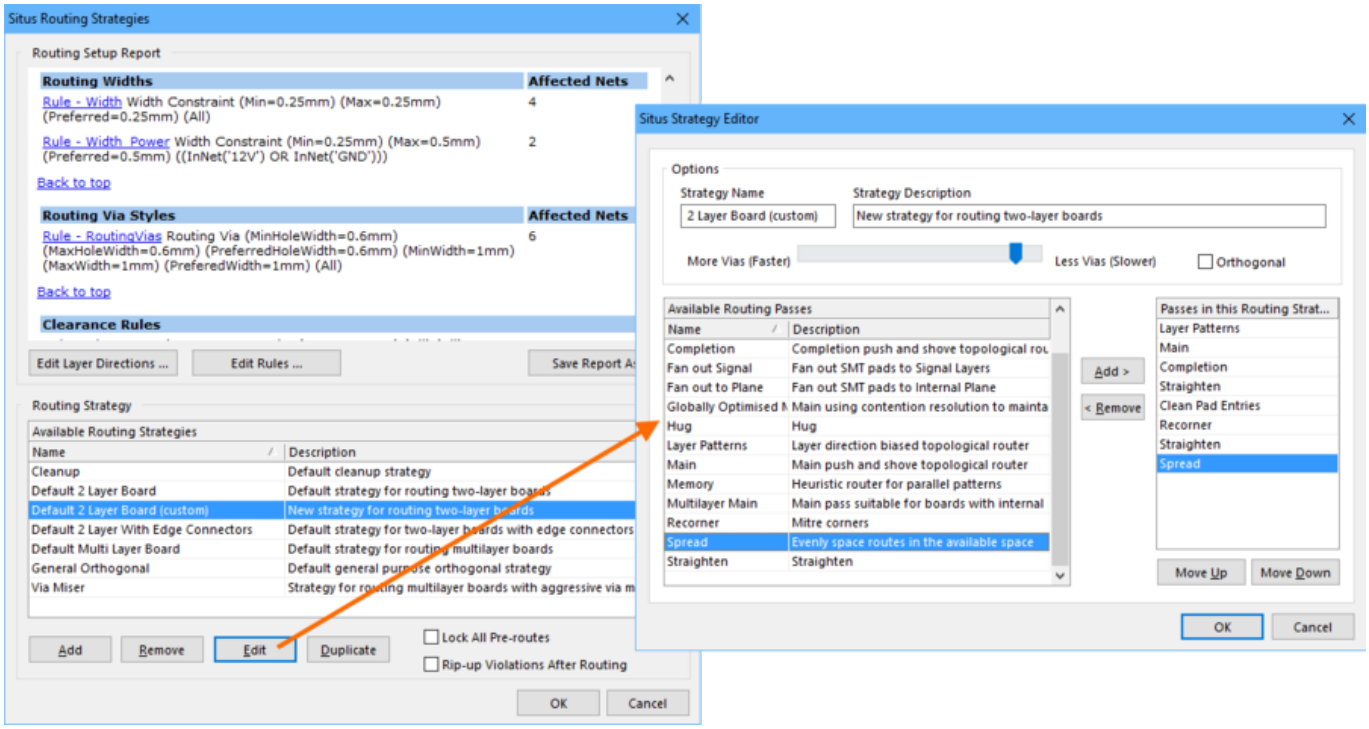
Configuring the Autorouter

Main articles: Situs Routing Strategies, Situs Strategy Editor

Altium Designer also includes a topological autorouter. A topological autorouter uses a different method of mapping the routing space - one that is not geometrically constrained. Rather than using workspace coordinate information as a frame of reference (dividing it into a grid), a topological autorouter builds a map using only the relative positions of the obstacles in the space, without reference to their coordinates.

Topological mapping is a spatial-analysis technique that triangulates the space between adjacent obstacles. This triangulated map is then used by the routing algorithms to "weave" between the obstacle pairs, from the start route point to the end route point. The greatest strengths of this approach are that the map is shape independent (the obstacles and routing paths can be any shape) and the space can be traversed at any angle - the routing algorithms are not restricted to purely vertical or horizontal paths, as with a rectilinear expansion routers.

Translating this into a user interface, the router has a number of different routing passes available; such as Fan Out to Plane, Main, Memory, Spread, Recorner, and so on. These are bundled together to create a Routing Strategy, which the designer can then run on their board. There are a number of pre-defined strategies already available in the *Routing Strategies* dialog, and new ones are easily created using the *Strategy Editor*.

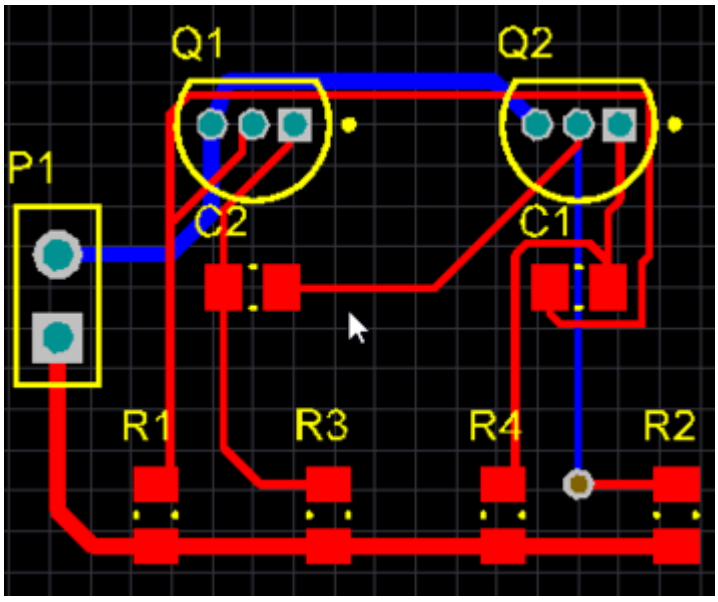


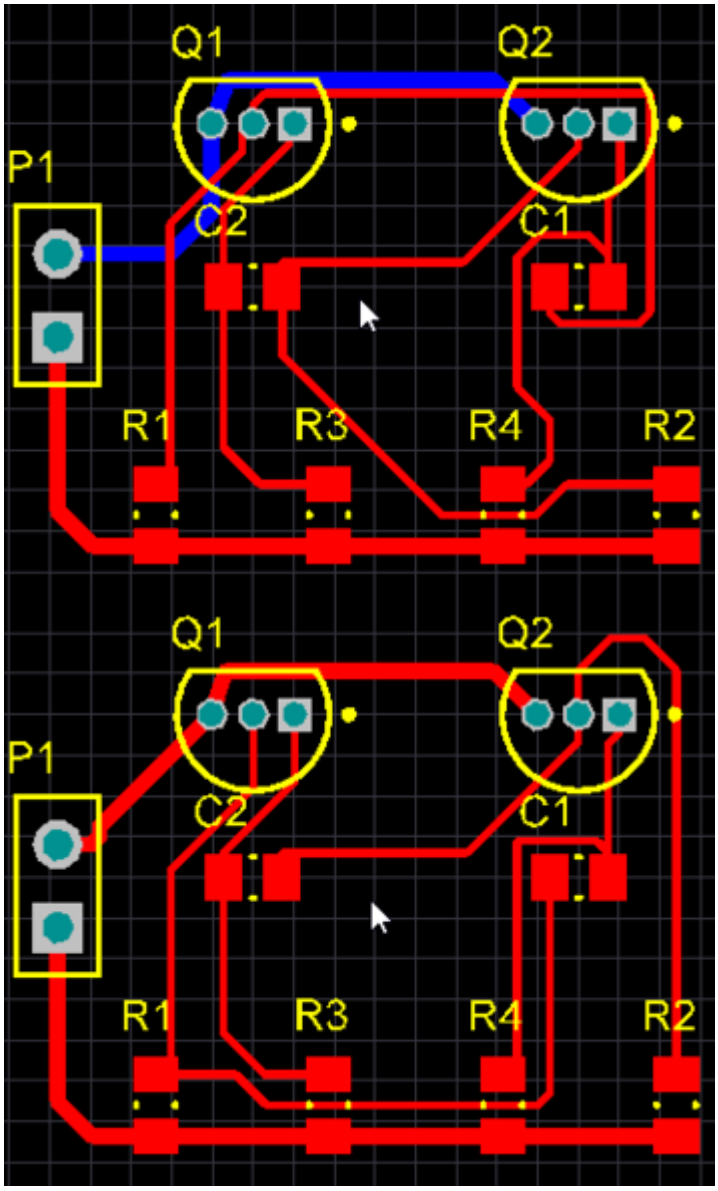
Select an existing routing strategy, or create a new one in the Strategy Editor. Note that the default strategies cannot be edited, duplicate one to explore the strategies.

Running the Autorouter

- The autorouter is configured and run from the **Route » Auto Route** submenu. Selecting **All** from the menu opens the *Routing Strategies* dialog, which is used to configure the strategies, select the required strategy, and run the autorouter.
- The autorouter will route on the layers allowed by the Routing Layers design rule, in the directions specified in the autorouter *Layer Directions* dialog (where possible).

The images below show the autorouting results using: the Default 2 Layer Board Strategy on the left; a user-defined strategy in the middle (the chosen routing passes are shown in the dialog image above); and that same strategy restricted to top layer only (by clicking the **Edit Layer Directions** button in the *Situs Routing Strategies* dialog, to disable the use of the bottom layer), on the right.





Autorouting results for the default 2 layer strategy (left image), a user-defined strategy (center image), and the same user-defined strategy limited to the top layer only.

Exploring the capabilities of the autorouter:

1. Un-route the board by running the **Route » Un-Route » All** command (shortcut: **U, U, A**).
2. Select **Route » Auto Route » All**. The *Situs Routing Strategies* dialog displays, the top region of the dialog displays the **Routing Setup Report**, warnings and errors are shown in red, *always* check for warnings/errors. The lower half of the dialog shows the available **Routing Strategies**, the selected one will be highlighted. For this board it should default to the **Default 2 Layer Board** strategy.
3. Click the **Route All** button in the *Routing Strategies* dialog. The *Messages* panel displays the process of the autorouting. Because it routes your board directly in the PCB editing window, there is no need to wrestle with exporting and importing route files.
4. To route the board single-sided, click the **Edit Layer Directions** button in the *Situs Routing Strategies* dialog, and modify the **Current Setting** field. Alternatively, you can modify the Routing Layers design rule.
5. An important point to make, the autorouter prefers a challenging board, often giving better results on a dense, more complex design than on a simple board. To improve the quality of the finished result, select **Autoroute » All** again, except this time select the **Cleanup** routing strategy. This strategy will attempt to straighten the routes, reducing the number of corners. You can run the Cleanup strategy multiple times if required. If nothing changes you might like

to interactively re-route a connection in a convoluted pattern, then try the Cleanup strategy.
6. If you want to keep the autorouting results, save your board. Otherwise use **Undo** or close/open to return the board to the required routed state.

Don't worry if the routing in your design is not exactly the same as shown in the figure above - because the component placement is not exactly the same, the routing will not be either.

Verifying Your Board Design

Main article: PCB Design Rules Reference

The PCB editor is a rules-driven board design environment, in which you can define many types of design rules that can be checked to ensure the integrity of your board. Typically you set up the design rules at the start of the design process. The on-line DRC feature will monitor the enabled rules as you work and immediately highlight any detected design violations. Alternatively, you can also run a batch DRC to test that the design complies with the rules, generating a report that details the enabled rules and any detected violations.

Earlier in the tutorial you examined the routing design rules, adding a new width constraint rule targeting the power nets, as well as an electrical clearance constraint and a routing via style rule. As well as these, there are a number of other design rules that are automatically defined when a new board is created.

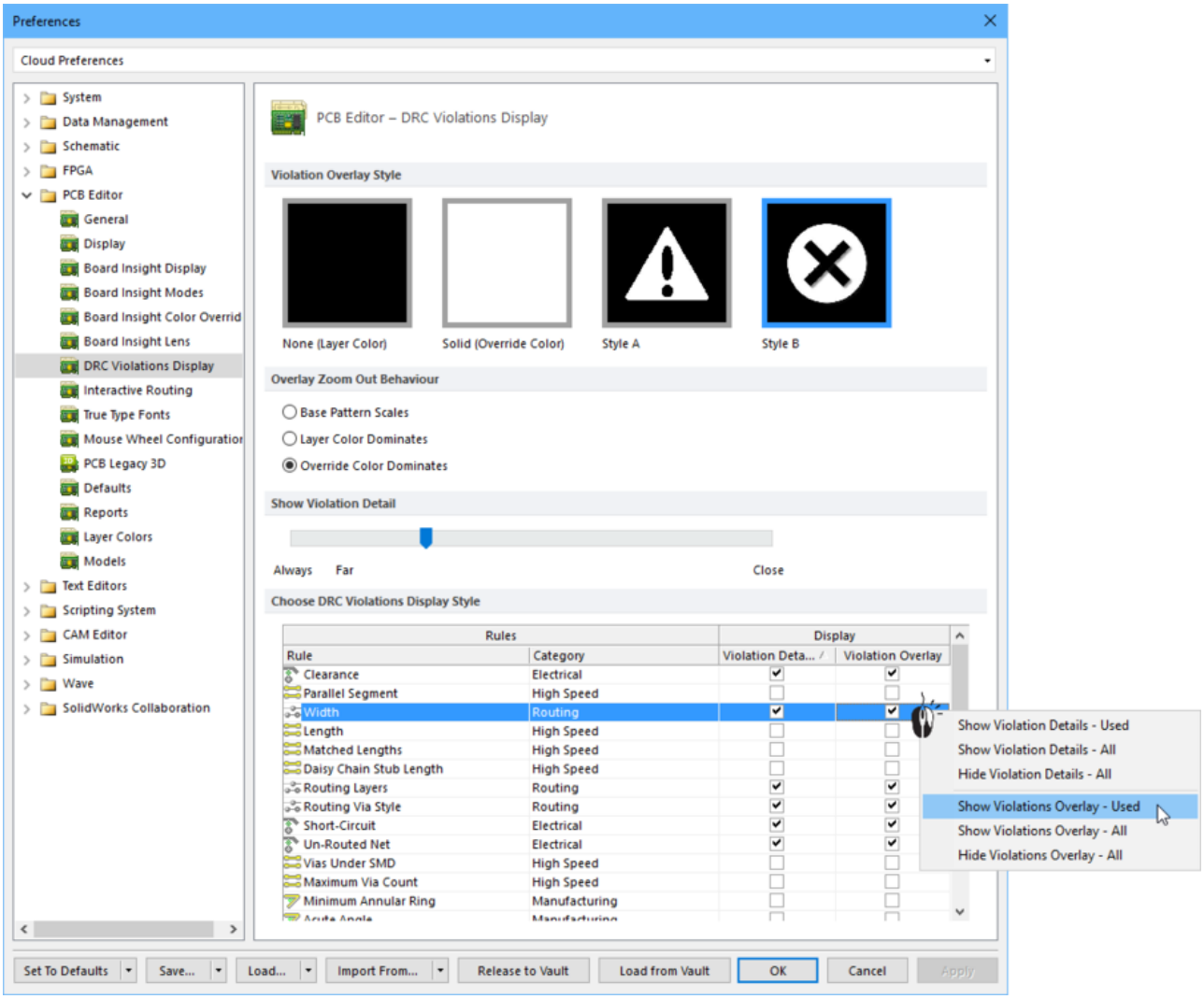
Configuring the Display of Rule Violations

Main article: PCB Editor - DRC Violations Display

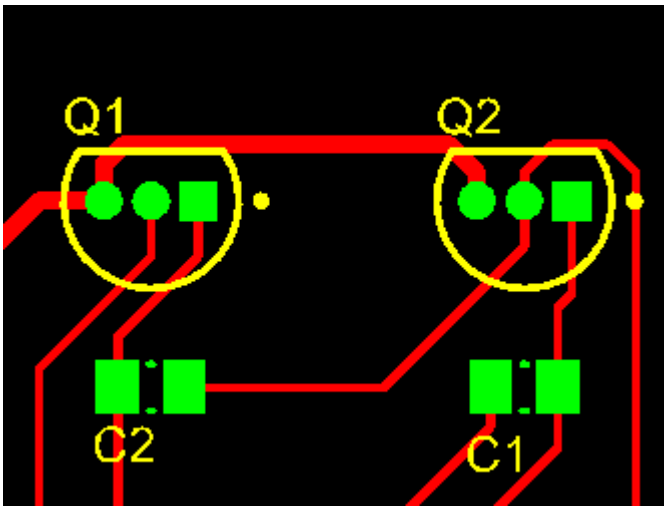
Before checking for rule violations, it is important to understand how violations are displayed.

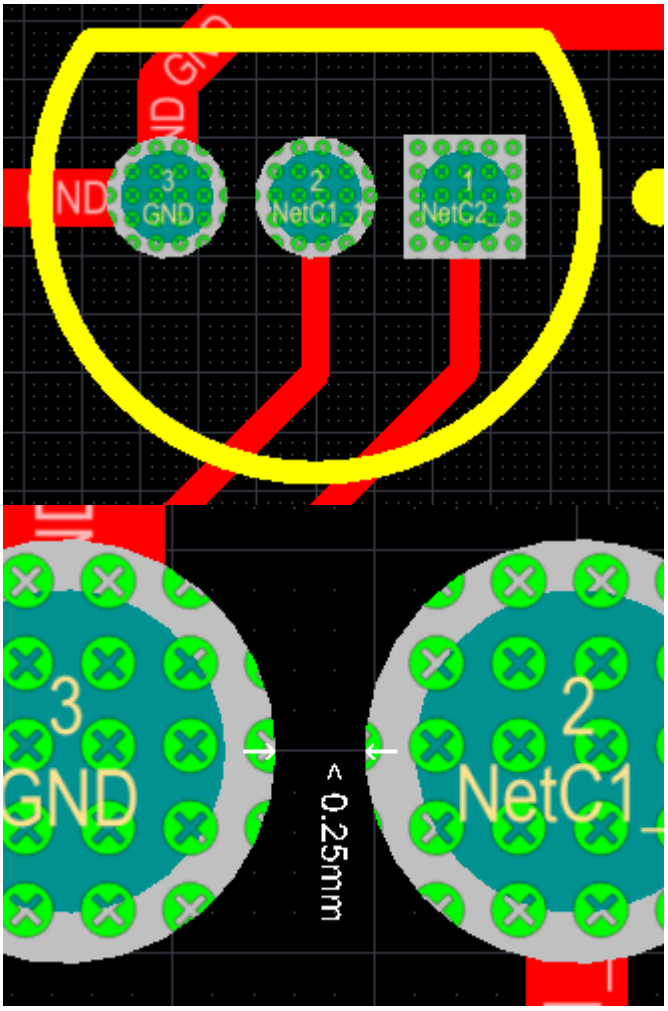
Altium Designer has two techniques for displaying design rule violations, each with their own advantages. These are configured in the **PCB Editor - DRC Violations Display** page of the *Preferences* dialog:

- **Violation Overlay** - Violations are identifed by the primitive-in-error being highlighted in the color chosen for the DRC Error Markers (configured in the *View Configurations* dialog, press **L** to open). The default behavior is to show the primitives in a solid color when zoomed out, changing to the selected **Violation Overlay Style** as you zoom it. The default is **Style B**, a circle with a cross in it.
- **Violation Details** - As you zoom further in **Violation Detail** is added (if enabled), detailing the nature of the error. Use the **Show Violation Detail** slider to define at what zoom level the Violation Details start to display. Enable the required **Display** options in the *Preferences* dialog.



Violations can be displayed as a colored overlay and also as a detailed message, with different symbols being used to show different detail of the error type.





Violations are shown in solid green (left image), as you zoom in this changes to the selected **Violation Overlay Style** (center image), as you zoom in further **Violation Details** are added.

[Preparing to run a Design Rule Check (DRC):]

1. Select **Design » Board Layers & Colors** (shortcut: **L**) and ensure that **Show** checkbox next to the **DRC Error Markers** option in the **System Colors** section is enabled (ticked) so that DRC error markers will be displayed.
2. Confirm that the **Online DRC** (Design Rule Checking) system is enabled, the checkbox is in the **PCB Editor - General** page of the *Preferences* dialog. Keep the *Preferences* dialog open, and switch to the **PCB Editor - DRC Violations Display** page of the dialog.
3. The **PCB Editor - DRC Violations Display** page of the *Preferences* dialog is used to configure how violations are displayed in the workspace. There are 2 different methods available for displaying violations, each with their own strengths.
4. For the tutorial, right-click in the **Display** area of the **PCB Editor - DRC Violations Display** page of the *Preferences* dialog and select **Show Violation Details - Used**, then right-click again and select **Show Violation Overlay - Used**, as shown in the dialog image above.
5. You are now ready to check the design for errors.

> When you create a new board, it will include default design rules that might not be needed for your design. For example, **Assembly** and **Fabrication Testpoint** type design rules are included when you create a new board, which are not needed in this design. Before proceeding to check the board for violations, open the *PCB Rules and Constraints Editor*, drill down to the **Testpoint** category and disable the 4 Testpoint type rules.

The rules that are needed will depend on the nature of your design, there is no specific set of rules that suits every design. Keep this in mind as you are checking rule violations, ask yourself do I need this rule to be enabled? If you're attempting to work out the function of a rule in the *PCB Rules and Constraints Editor* and are unsure, click anywhere in the constraints area of the rule and press **F1** for more information about that specific rule.

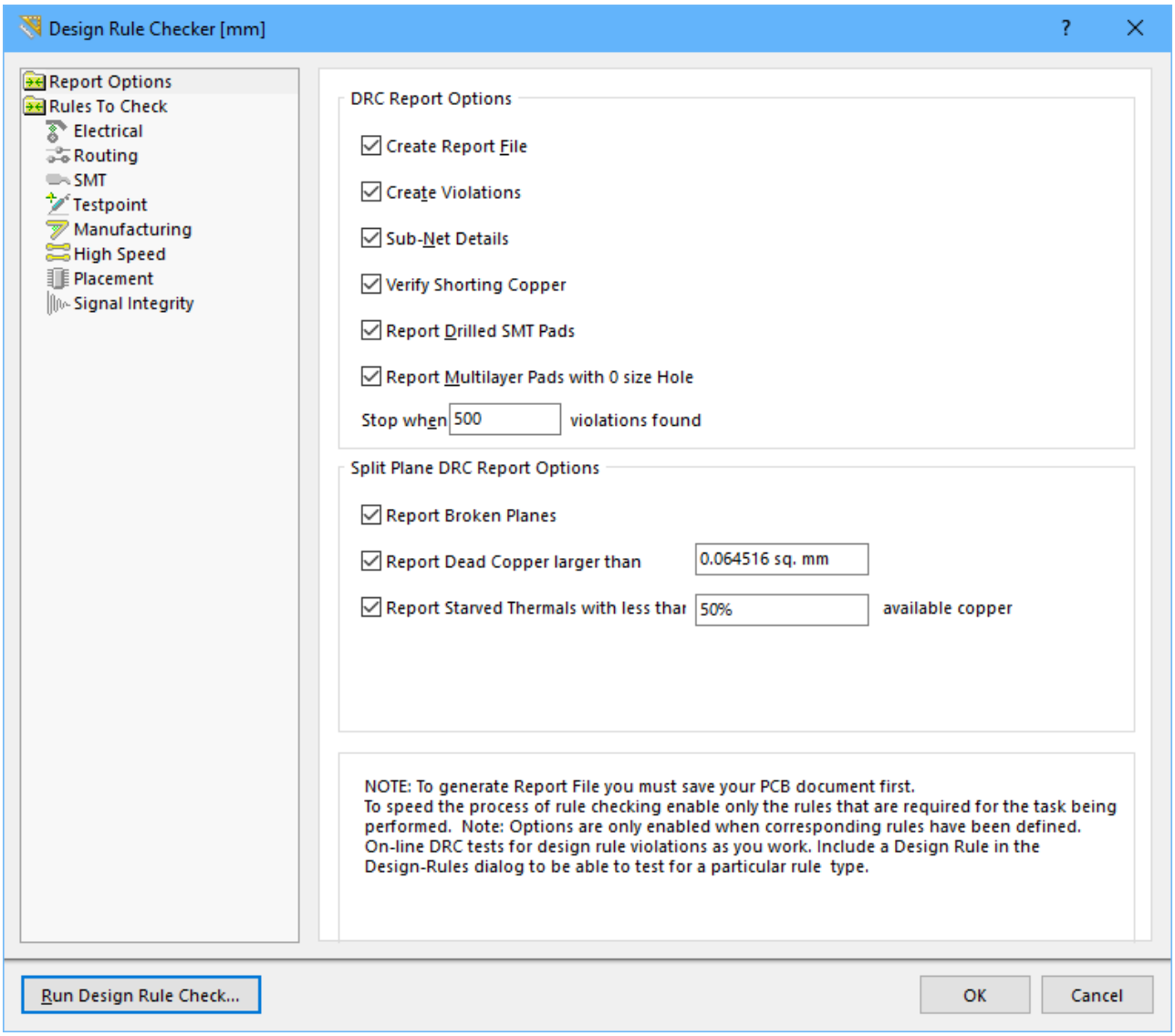
Configuring the Rule Checker

Main article: Design Rule Checker

The design is checked for violations by running the Design Rule Checker. Run the **Tools » Design Rule Check** command to open the dialog. Both online and batch DRC are configured in this dialog.

DRC Report Options

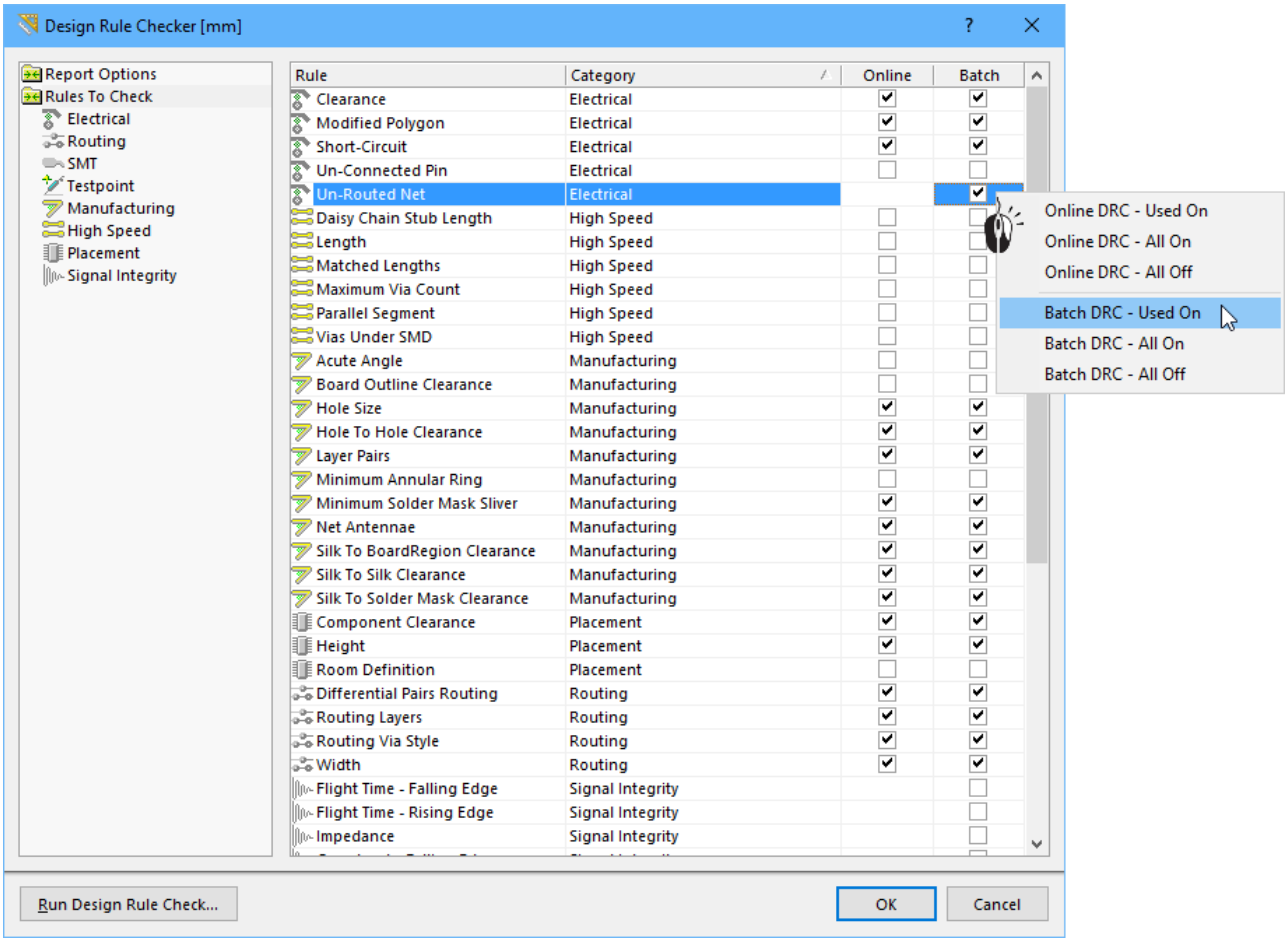
- By default, the dialog opens showing the **Report Options** page selected in the tree on the left of the dialog (shown below).
- The right side of the dialog displays a list of general reporting options, for more information about the options press **F1** when the cursor is over the dialog. These options can be left at their defaults.



Rule checking, both online and batch, is configured in the Design Rule Checker dialog.

DRC Rules to Check

- The testing of specific rules is configured in the **Rules to Check** section of the dialog, select this page in the tree on the left of the dialog to list all of the rule types (shown below). You can also examine them by type, for example **Electrical**, by selecting that page on the left of the dialog.
- For most rule types there are checkboxes for **Online** (check as you work) and **Batch** (check this rule when the **Run Design Rule Check** button is clicked).
- Click to enable/disable the rules as required. Alternatively, right-click to display the context menu. This menu allows you to quickly toggle the **Online** and **Batch** settings, select the **Batch DRC - Used On** entry, as shown in the image below.



Checking is configured for each rule type, use the right-click menu to enable the Used design rules.

Running a Design Rule Check (DRC)

Click the **Run Design Rule Check** button at the bottom of the dialog to perform a design rule check. When the button is clicked the DRC will run, then:

- The *Messages* panel will appear, listing all detected errors.
- If the Create Report File option was enabled in the Report Options page of the dialog, a **Design Rule Verification Report** will open in a separate document tab, the report for the tutorial is shown below.
    - The upper upper section of the report details the rules that are enabled for checking and the number of detected violations, click on a rule to jump down the report and examine those errors.
    - Below the summary of violating rules are specific details about each violation.
    - The links in the report are live, click on a specific error to jump back to the board and

examine that error on the board. Note that the zoom level for this click action is configured in the **System - Navigation** page of the *Preferences* dialog, experiment to find a zoom level that suits you.

Altium Designer

Design Rule Verification Report

Date:	21-Apr-16		
Time:	2:45:38 PM	**Warnings:**	0
Elapsed Time:	00:00:01	**Rule Violations:**	18
Filename:	C:\Designs\Multivibrator\Multivibrator.PcbDoc		

Summary

Warnings	Count
Total	**0**

Rule Violations	Count
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mm) (All)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=0.25mm) (All),(All)	2
Silk To Solder Mask (Clearance=0.25mm) (IsPad),(All)	8
Minimum Solder Mask Sliver (Gap=0.25mm) (All),(All)	4
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm) and Width Constraints (Min=0.381mm) (Max=0.381mm) (Prefered=0.381mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.5mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm) (All),(All)	0
Routing Via (MinHoleWidth=0.6mm) (MaxHoleWidth=0.6mm) (PreferredHoleWidth=0.6mm) (MinWidth=1mm) (MaxWidth=1mm) (PreferedWidth=1mm) (All)	0
Routing Layers(All)	0
Width Constraint (Min=0.25mm) (Max=0.25mm) (Preferred=0.25mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All)	0
Clearance Constraint (Gap=0.25mm) (All),(All)	4
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Width Constraint (Min=0.25mm) (Max=0.5mm) (Preferred=0.5mm) ((InNet('12V') OR InNet('GND')))	0
Total	**18**

The upper section in the report details the rules that are enabled for checking and the number of detected violations, click on a rule to jump down the report and examine those errors.

Silk to Silk (Clearance=0.25mm) (All),(All)	
Text "C2" (8.235mm,16.562mm) Top Overlay	Arc (10mm,20mm) Top Overlay
Text "C1" (18.235mm,16.562mm) Top Overlay	Arc (20mm,20mm) Top Overlay

Back to top

Silk To Solder Mask (Clearance=0.25mm) (IsPad),(All)	
Track (19.95mm,14.375mm)(20.05mm,14.375mm) Top Overlay	Pad C1-1(19.1mm,15mm) Top Layer
Track (19.95mm,15.625mm)(20.05mm,15.625mm) Top Overlay	Pad C1-1(19.1mm,15mm) Top Layer
Track (19.95mm,14.375mm)(20.05mm,14.375mm) Top Overlay	Pad C1-2(20.9mm,15mm) Top Layer
Track (19.95mm,15.625mm)(20.05mm,15.625mm) Top Overlay	Pad C1-2(20.9mm,15mm) Top Layer
Track (9.95mm,14.375mm)(10.05mm,14.375mm) Top Overlay	Pad C2-1(9.1mm,15mm) Top Layer
Track (9.95mm,15.625mm)(10.05mm,15.625mm) Top Overlay	Pad C2-1(9.1mm,15mm) Top Layer
Track (9.95mm,14.375mm)(10.05mm,14.375mm) Top Overlay	Pad C2-2(10.9mm,15mm) Top Layer
Track (9.95mm,15.625mm)(10.05mm,15.625mm) Top Overlay	Pad C2-2(10.9mm,15mm) Top Layer

Back to top

Minimum Solder Mask Sliver (Gap=0.25mm) (All),(All)	
Pad Q2-2(20mm,20mm) Multi-Layer	Pad Q2-1(21.27mm,20mm) Multi-Layer
Pad Q2-3(18.73mm,20mm) Multi-Layer	Pad Q2-2(20mm,20mm) Multi-Layer
Pad Q1-2(10mm,20mm) Multi-Layer	Pad Q1-1(11.27mm,20mm) Multi-Layer
Pad Q1-3(8.73mm,20mm) Multi-Layer	Pad Q1-2(10mm,20mm) Multi-Layer

Back to top

Clearance Constraint (Gap=0.25mm) (All),(All)	
Pad Q2-2(20mm,20mm) Multi-Layer	Pad Q2-1(21.27mm,20mm) Multi-Layer
Pad Q2-3(18.73mm,20mm) Multi-Layer	Pad Q2-2(20mm,20mm) Multi-Layer
Pad Q1-2(10mm,20mm) Multi-Layer	Pad Q1-1(11.27mm,20mm) Multi-Layer
Pad Q1-3(8.73mm,20mm) Multi-Layer	Pad Q1-2(10mm,20mm) Multi-Layer

Back to top

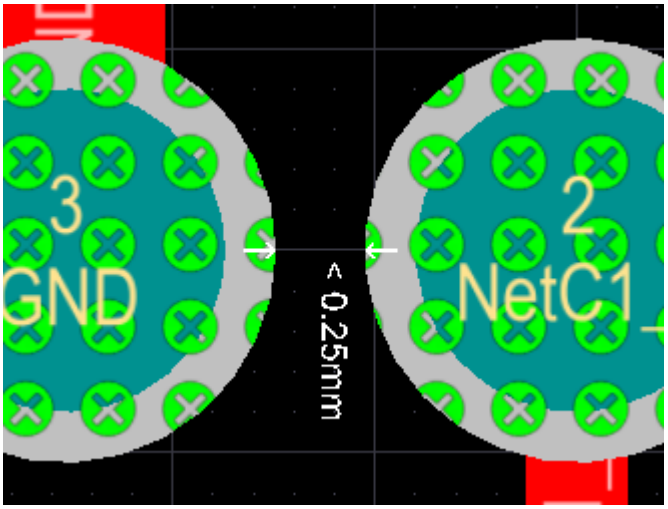
The lower section of the report shows each rule that is being violated, followed by a list of the objects in error. Click on an error to jump to that object on the PCB.

Locating the Error Condition

When you are new to the software, a long list of violations can initially seem overwhelming. A good approach to managing this is to disable and enable rules in the *Design Rule Check* dialog, at different stages of the design process. It is not advisable to disable the design rules themselves if there are violations, just the checking of them. For example, you would always disable the **Un-Routed Net**

check until the board is fully routed.

- When a batch DRC is run on the tutorial board, there are:
  - 2 Silk to Silk clearance errors - the distance between two adjacent sections of silkscreen is less than allowed by this rule.
  - 8 Silk to Solder Mask clearance errors - the distance from the opening in the solder mask to the edge of a silkscreen object is less than allowed by this rule.
  - 4 Minimum Solder Mask Sliver errors - the minimum width of a strip of solder mask is less than allowed by this rule. This typically occurs between component pads.
  - 4 clearance constraint violations - the measured electrical clearance value between objects on signal layers is less than the minimum amount specified by this rule.
- To locate a violation:
  - click the link in the report file, or
  - double click in the *Messages* panel,
  - click on a violation in the *PCB Rules and Violations* panel.
- Using the Violation Details, you can establish the error condition.
- The image below shows the Violation Details for one of the clearance constraint errors, indicated by the white arrows and the `0.25mm` text, indicating that this gap is less than the minimum `0.25mm` allowed by the rule. The next step is to work out what the actual value is so you know how much it has failed by, and can then decide how to resolve this error.



The Violation Details show that the clearance between these 2 pads is less that 0.25mm, it does not detail the actual clearance though.

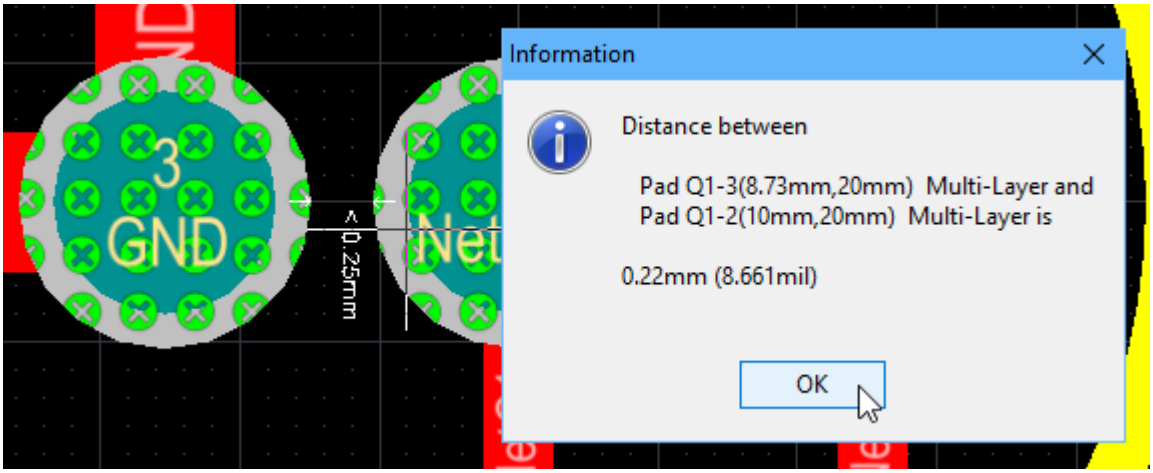
Understanding the Error Condition

So you've found an error, how do you know how much it has failed by? As the designer you need this essential information, to be able to decide how best to resolve the error.

For example, if the rule says the allowable minimum solder mask sliver is 0.25 mm and the actual sliver is 0.24, then the situation is not that bad and you may be able to adjust the rule setting to accept this value. But if the actual sliver value is 0.02, then that is probably not a situation that can be resolved by adjusting the rule setting.

> The PC editor includes three handy measurement tools, **Measure Distance**, **Selected Primitives** and **Between Primitives**, available in the **Reports** menu.
>
> - **Measure Distance** - measure the distance between the 2 locations you click after

running the command, keep an eye on the Status bar for instructions. The location that you can click is constrained by the current snap grid.
- **Selected Primitives** - measure the length of selected tracks and arcs. Use this to work out route lengths, select the required objects manually, or use the **Select » Physical Connection** or **Select » Connected Copper** commands.
- **Between Primitives** - measure the edge-to-edge distance between the 2 primitives you click on after running the command, keep an eye on the Status bar for instructions.



Measuring the distance between the edges of adjacent pads, using the Measure Primitives command.

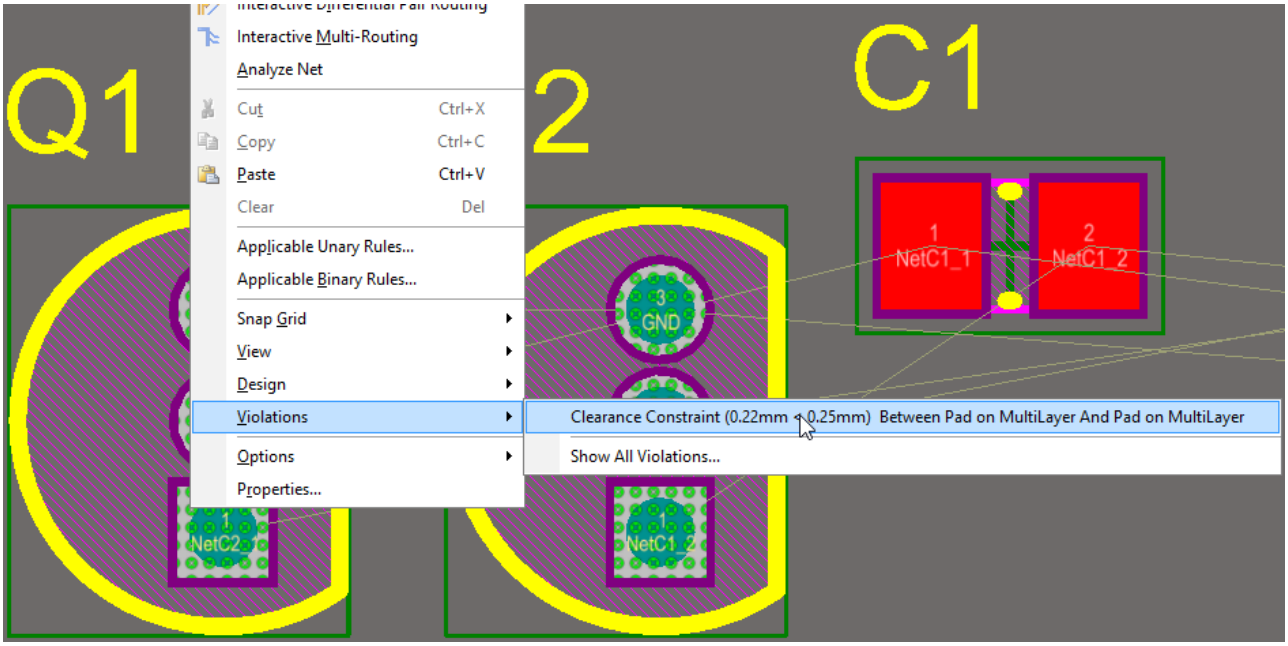
Apart from actually measuring the distance, there are a number of approaches to finding out how much a rule has failed by. You can use:

- the right-click **Violations** submenu, or
- the *PCB Rules and Violations* panel, or
- the detail included in the *Messages* panel - the actual value is detailed along with the specified value (for example, 0.175 < 0.254).

The Violations Submenu

The right-click **Violations** submenu was described earlier in the Existing Design Rule Violation section.

- The image below shows how the **Violations** submenu details the measured condition against the value specified by the rule.



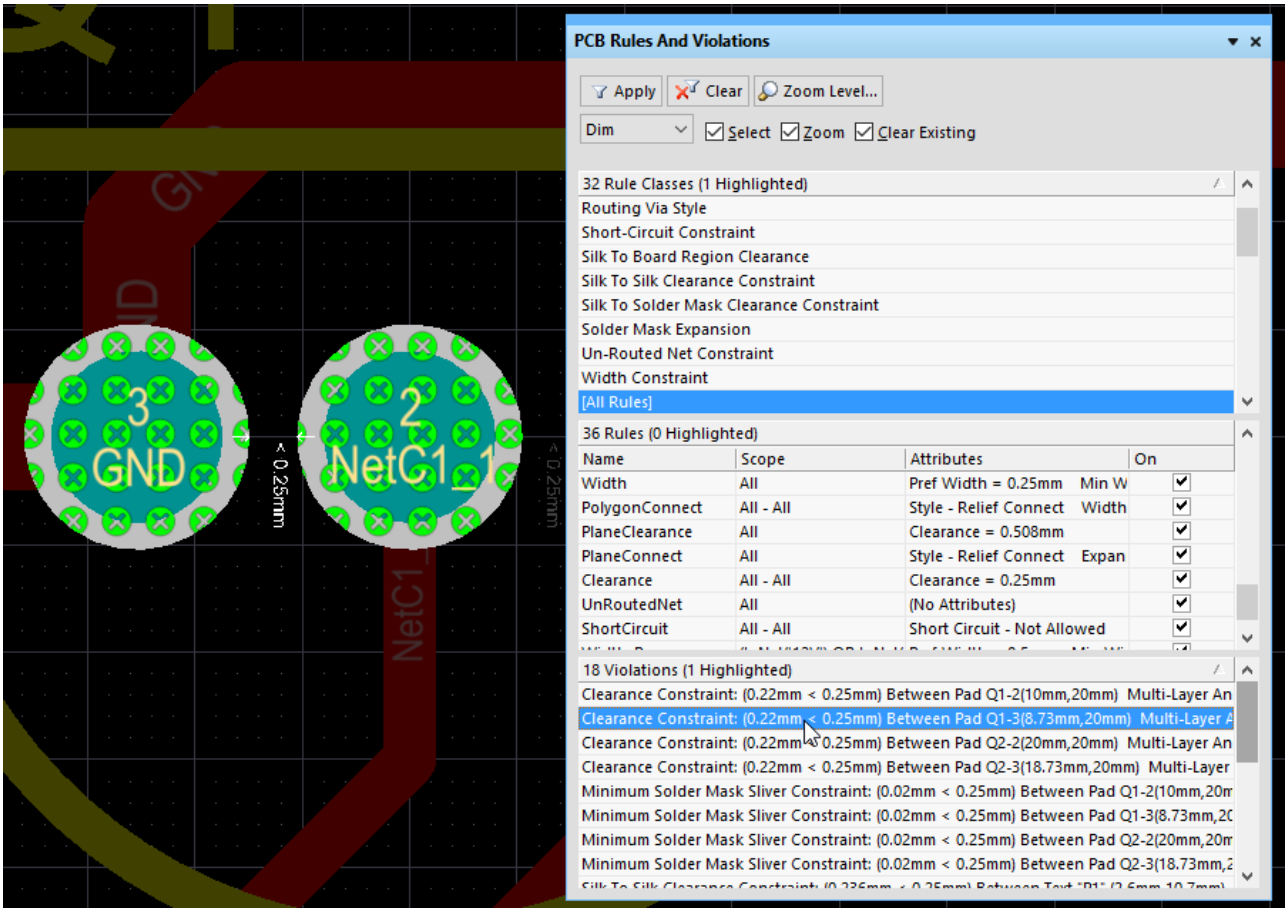
Right-click on a violation to examine what rule is being violated, and the violation conditions.

The PCB Rules and Violations Panel

Main article: PCB Rules and Violations Panel

The *PCB Rules and Violations* panel is an excellent feature for locating and understanding error conditions.

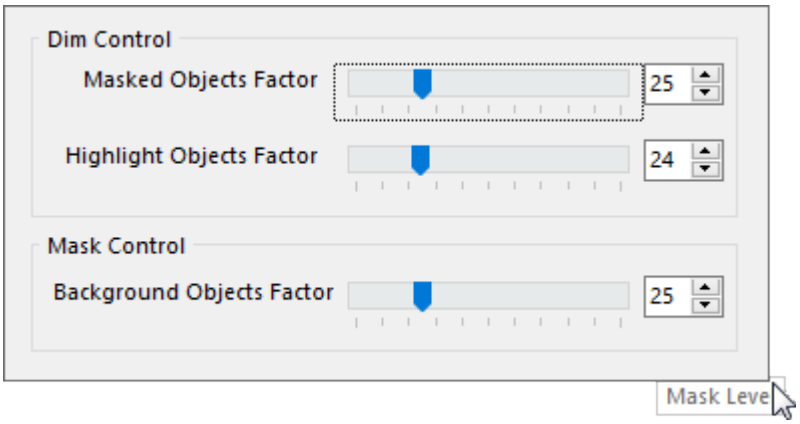
- Click the PCB button and select **Rules and Violations** from the menu to display the panel. It will default to show `[All Rules]` in the **Rule Classes** list. Once you have identified a rule type of interest, select that specific rule class so that only those violations are shown at the bottom of the panel.
- Click once on a violation in the list to jump to that violation on the board, double-click on a violation to open the *Violation Details* dialog.



The panel details the violation type, the measured value, the rule setting and the objects that are in violation.

Note that at the top of the *PCB Rules and Violations* panel there is a drop-down, which can be used to select **Normal**, **Dim** or **Mask**. Dim and Mask are display filter modes, where everything other than the object(s) of interest are faded, leaving only the chosen object(s) at normal display strength. The Dim mode applies the filter but still allows all workspace objects to be edited, the Mask mode filters out all other workspace objects, only allowing the unfiltered object(s) to be edited.

The amount that the display is faded is controlled by the **Dim** and **Mask** slider controls, click the **Mask Level** button down the bottom right to display the sliders. Experiment with these when you have the Mask mode or Dim mode applied.



To clear the filter you can either click the **Clear** button (next to the Mask Level button), or press the **Shift+C** shortcut. This filtering feature is very effective in a busy workspace, and can also be used in the *PCB* panel and the *PCB Filter* panel.

Resolving the Violations

As the designer you have to work out the most appropriate way of resolving each design rule violation. Let's start with the solder mask errors as they are related, and both error conditions may be affected by the changes you make to solder mask settings.

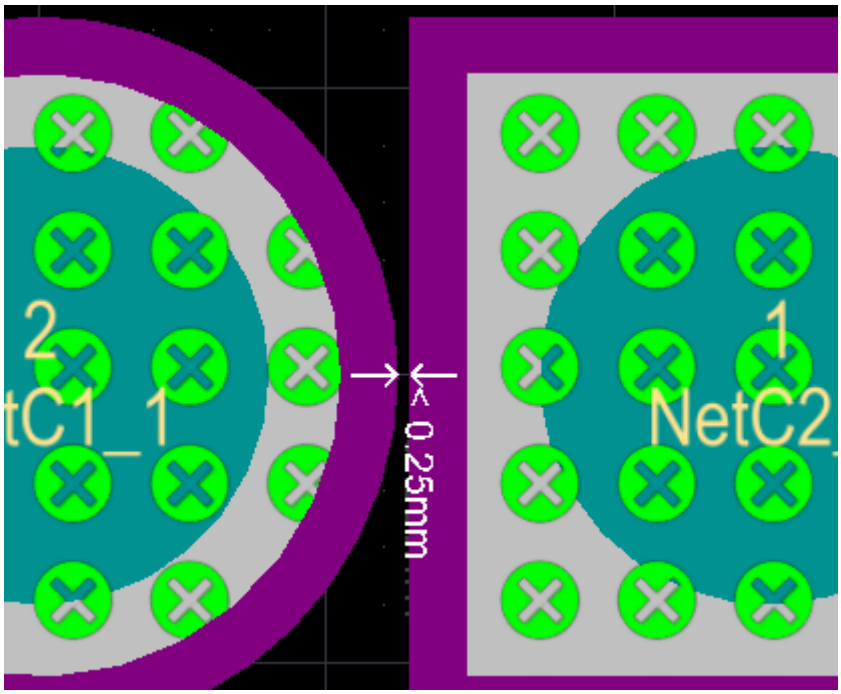
Solder Mask Errors

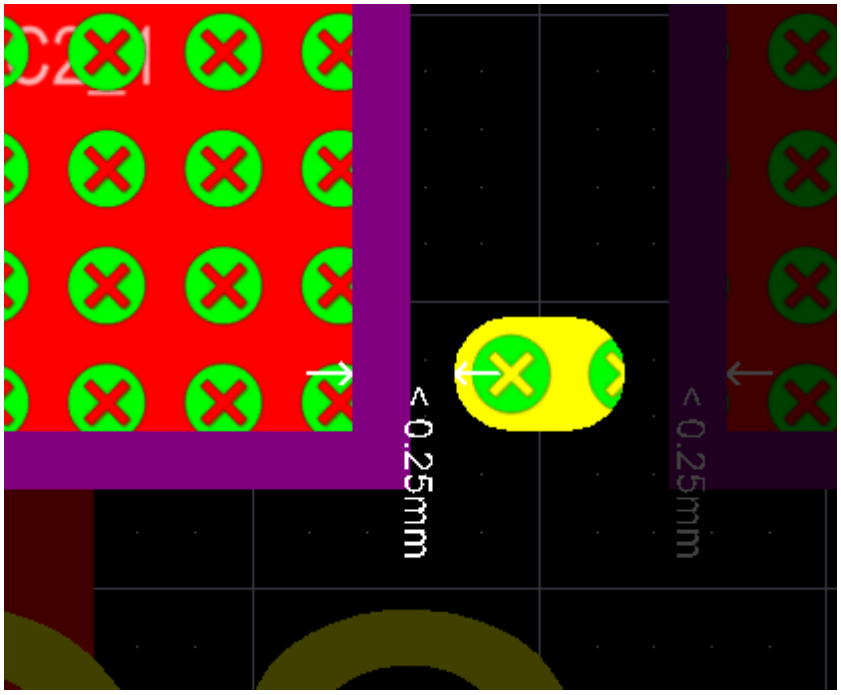
Main articles: Minimum Solder Mask Sliver, Silk to Solder Mask Clearance

The solder mask is a thin, lacquer-like layer applied to the outer surface of the board, providing a protective and insulating covering for the copper. Opening are created in the mask for components and wires to be soldered to the copper, it is these openings that are displayed as objects on the solder mask layer in the PCB editor (note that the solder mask layer is defined in the negative - the objects you see become holes in the actual solder mask).

During fabrication, solder mask is applied using different techniques, the lowest cost approach is to silkscreen it onto the board surface through a mask. To allow for layer alignment issues, the mask openings are typically larger than the pads, reflected by the 4mil (0.1mm) expansion value used in the default design rule.

There are other techniques for applying solder mask which offer higher-quality layer registration and more accurate shape definition, if these techniques are used the solder mask expansion can be smaller or even zero. Reducing the mask opening reduces the chance of having solder mask slivers or silk to solder mask clearance errors.





A solder mask sliver error shown on the left and a silk to solder mask clearance error on the right, the purple represents the solder mask expansion around each pad.

Errors such as these solder mask issues cannot be resolved without consideration of the fabrication technique that will be used to make the finished board.

For example, if this was a complex, multi-layer board for a high-value product, then it is likely that a high quality solder mask technology would be employed, which would allow a small or zero solder mask expansion. However, for a simple double-sided board like the tutorial it is more likely it will be targetting a low-cost product, requiring a low-cost solder mask technology to be used. That means resolving the solder mask sliver errors by reducing the solder mask expansion for the entire board is not a realistic solution.

Like many aspects of PCB design, the solution lies in making thoughtful trade-offs in a focused way, to minimize their impact.

Resolving the Solder Mask Sliver violations:

To resolve this violation you can:

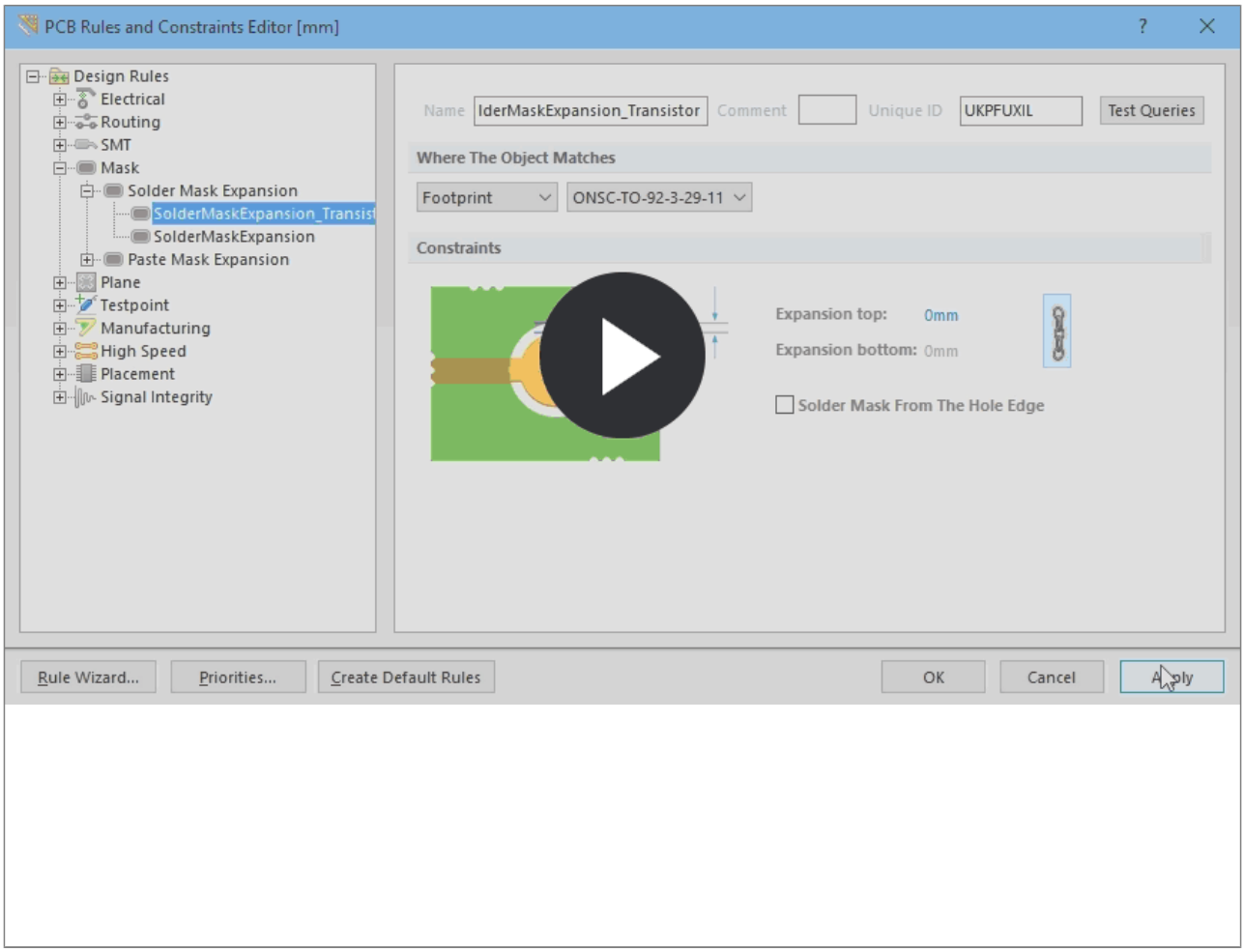
1. Increase the solder mask opening to completely remove the mask between the transistor pads, or
2. Decrease the minimum acceptable sliver width, or
3. Decrease the mask opening to widen the sliver to an acceptable width.

This is a design decision which would be made in light of your knowledge of the component, and the fabrication and assembly technology that is going to be used. Opening the mask to completely remove the mask between the transistor pads means that there is more chance of creating solder bridges between those pads, whereas decreasing the mask opening will still leave a sliver, which may or may not be acceptable, and will also introduce the possibility of mask-to-pad registration problems.

For this tutorial you will do a combination of the second and third options, decreasing the minimum sliver width to a value suitable for the settings being used on this board, and also decreasing the mask expansion, but only for the transistor pads.

1. The first step is to reduce the allowable sliver width. To do this, open the *PCB Rules and Constraints Editor*, then in the **Manufacturing** section locate and select the existing **Minimum Solder Mask Sliver** rule, called **MinimumSolderMaskSliver**.
2. A value equal to the pad separation of `0.22mm` (≈ 8.7mil) will be acceptable for a design such as this, edit the **Minimum Solder Mask Sliver** value to be `0.22mm` in the **Constraints** region of the rule.
3. Now click on **Mask** in the tree on the left of the dialog to show the current **Solder Mask Expansion** rules, there should be one rule, called **SolderMaskExpansion**.
4. Click on it to select the rule and display its settings, it will specify an expansion value of `0.102mm` (4mil). Since it is only the transistor pads that are in violation you will not edit this value, instead you will create a new rule.
5. To add a new Solder Mask Expansion rule, right-click on the rule and select **New Rule** from the menu. A new rule called **SolderMaskExpansion_1** will be created, click on it to display its settings.
6. Edit the rule settings to be as shown below:

    - **Name** - SolderMaskExpansion_Transistor
    - **Full Query** - HasFootprint('ONSC-TO-92-3-29-11') (the name of the transistor footprint)
    - **Expansion** - 0mm



You can use the Query Builder to help create the new rule.

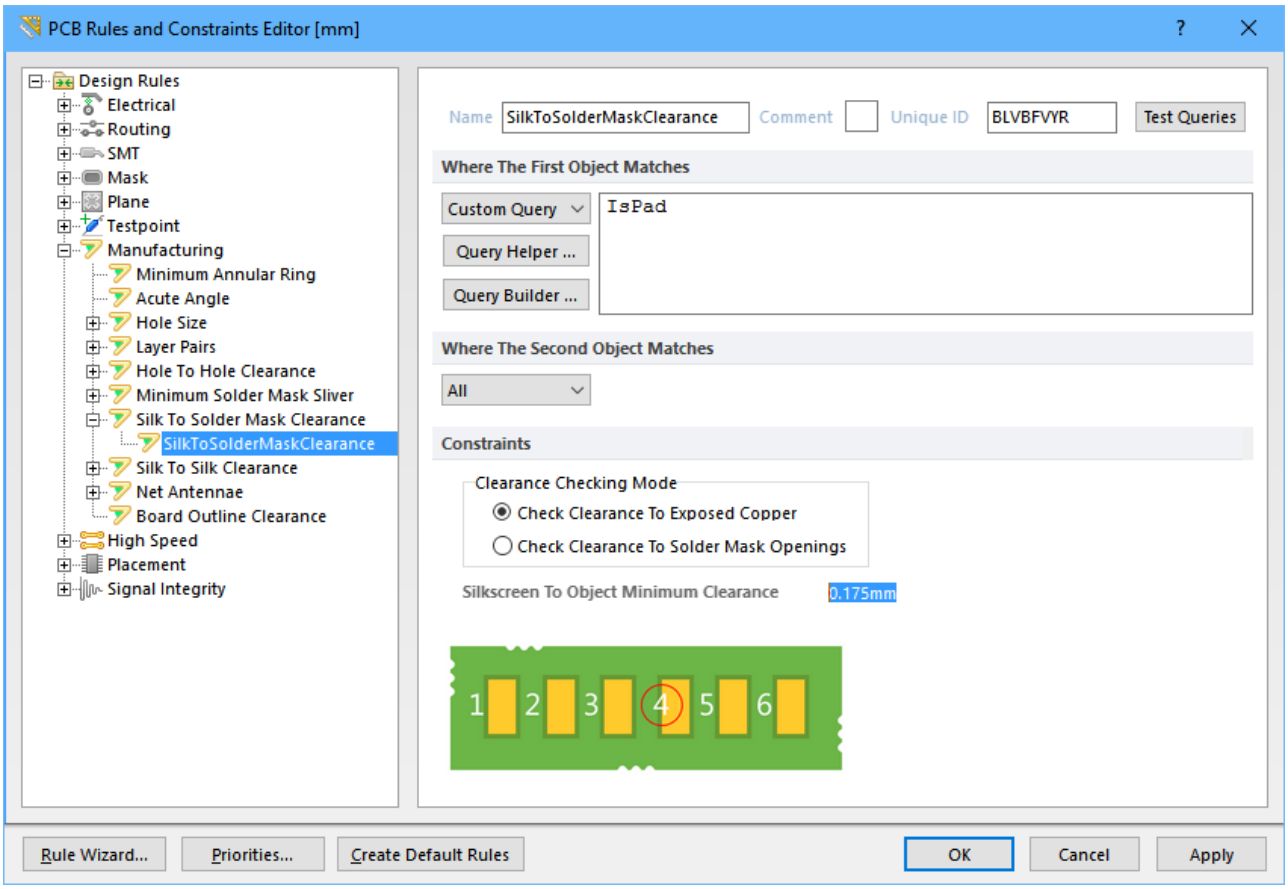
6. Click **Apply** to accept the changes and keep the *PCB Rules and Constraints Editor* open.

[Resolving the Silk to Solder Mask Clearance violations:]

The function of this rule is to ensure there is sufficient separation between the silkscreen objects and

the copper. The rule supports checking against the opening in the mask, or checking against the copper exposed by that opening in the mask.

1. For this violation, the actual measurement is close to the current rule setting, 0.175mm versus 0.25mm, as can be seen in the *Messages* or the *PCB Rules and Violations* panels. The value 0.175mm is still an acceptable separation, edit the constraint value, as shown in the image below.



Edit the clearance to be 0.175mm.

2. Click **OK** to accept the changes and close the *PCB Rules and Constraints Editor*.

Clearance Violations

Main article: Clearance Constraint

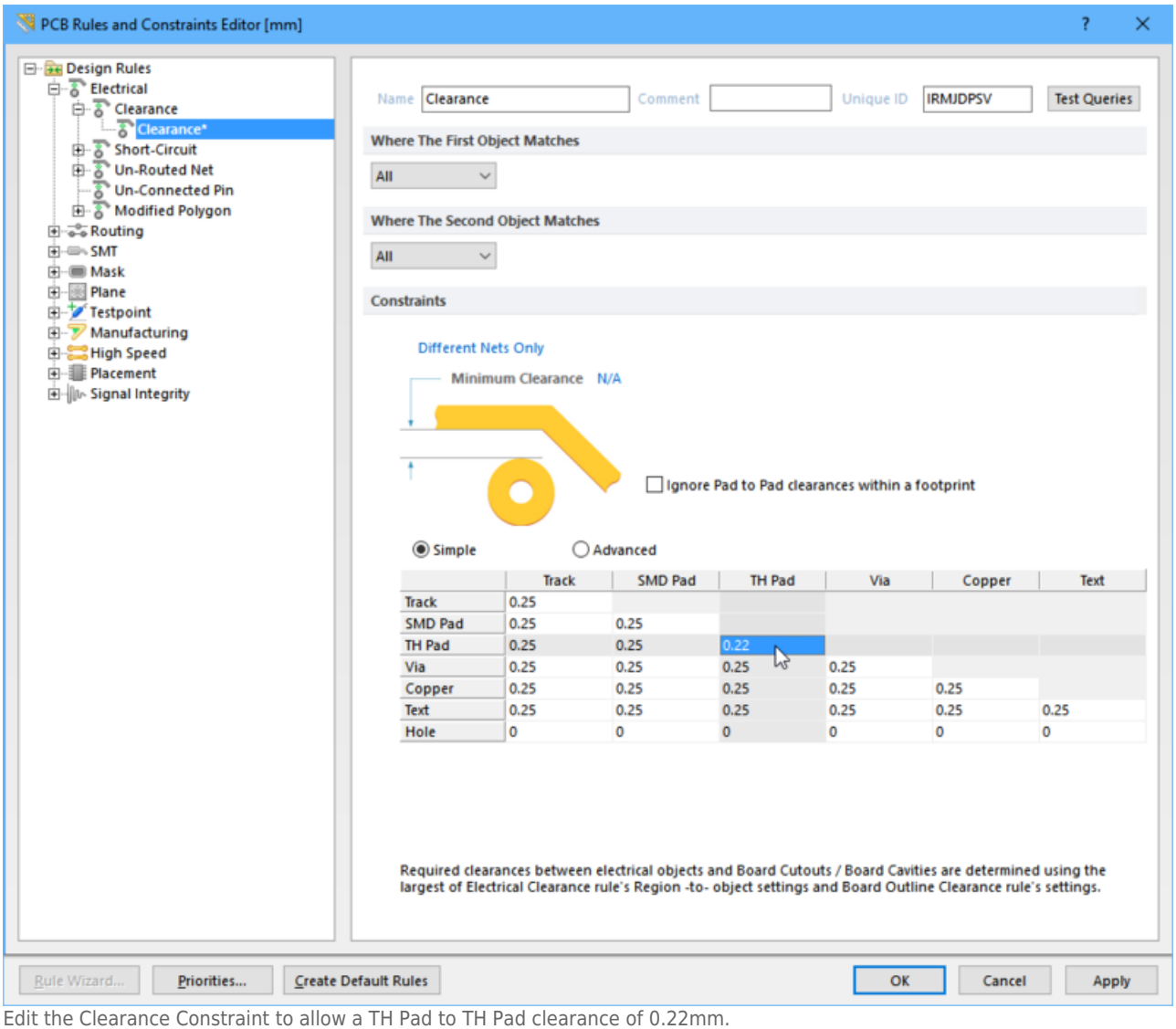
There are two ways of resolving this clearance constraint:

- Decrease the size of the transistor footprint pads to increase the clearance between the pads, or
- Configure the rules to allow a smaller clearance between the transistor footprint pads.

Since the 0.25mm clearance is quite generous and the actual clearance is quite close to this value (0.22mm), a good choice in this situation would be to configure the rules to allow a smaller clearance. This can be done in the existing Clearance Constraint design rule, as shown below.

- The TH Pad - to - TH Pad value is changed to `0.22mm` in the grid region of the rule constraint. To edit a cell first select it, then press **F2**.
- This solution is acceptable in this situation because the only other component with thruhole

pads is the connector, which has pads spaced over 1mm apart. If this was not the case, the best solution would be to add a second clearance constaint targetting just the transistor pads, as was done for the solder mask expansion rules.



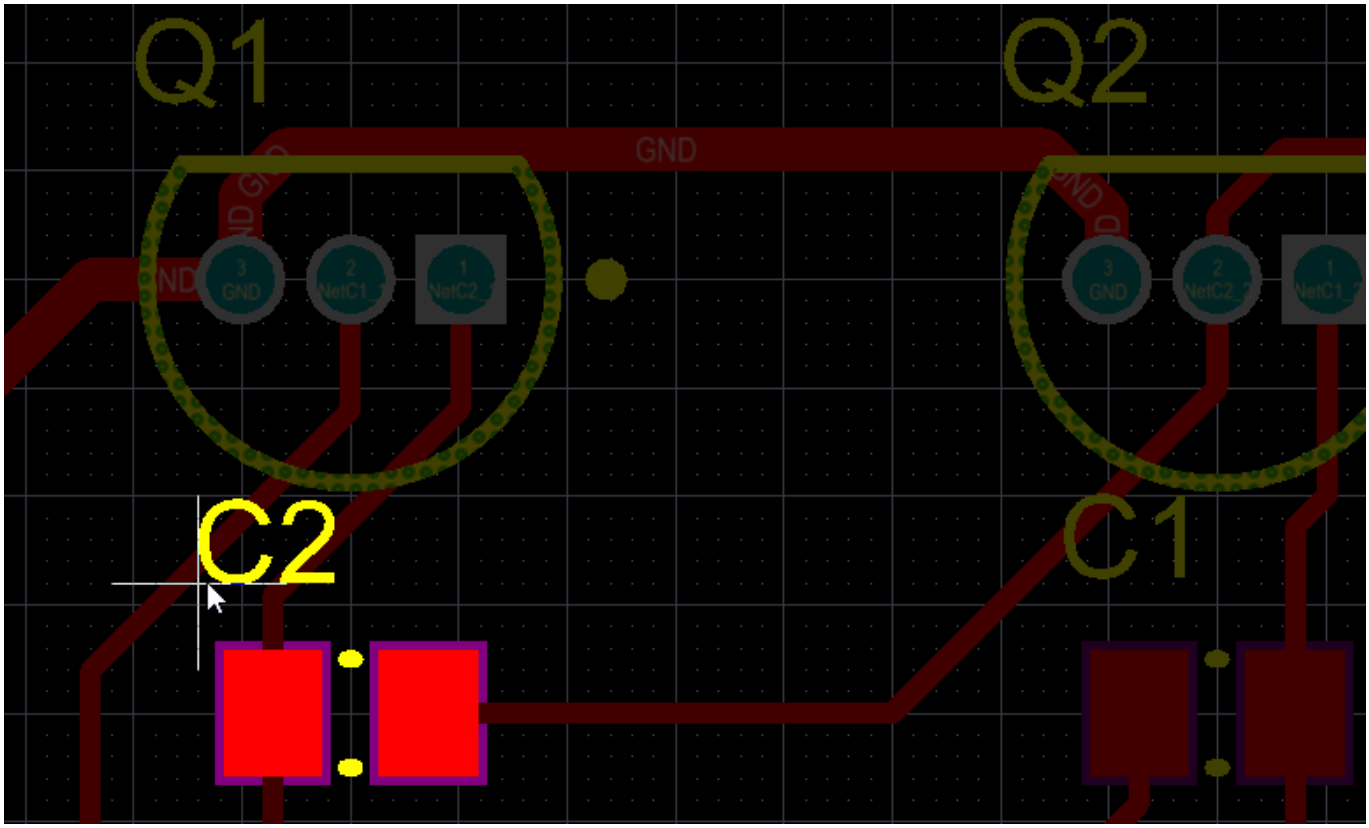
Edit the Clearance Constraint to allow a TH Pad to TH Pad clearance of 0.22mm.

Silk to Silk Clearance Violation

Main article: Silk to Silk Clearance

The last error to resolve is the silk to silk clearance violations. These are usually caused by a designator being too close to the outline of an adjacent component. You design may not have any of these violations - it depends on how close you placed the components, or if you have already repositioned the designators. Click and hold on a designator to move it - all objects will dim apart from the objects in the component whose designator is being moved - move that designator to a new location.

Designator movement will be constrained by the current snap grid, if it is currently too coarse press **Ctrl+G** and enter a new grid value.



Reposition any designator that is causing a silk to silk violation.

> Always confirm that you have a clean Design Rule Verification Report before generating outputs.

Well done! You have completed the PCB layout and are ready to produce output documentation. Before doing that, let's explore the PCB editor's 3D capabilities.

Viewing Your Board in 3D

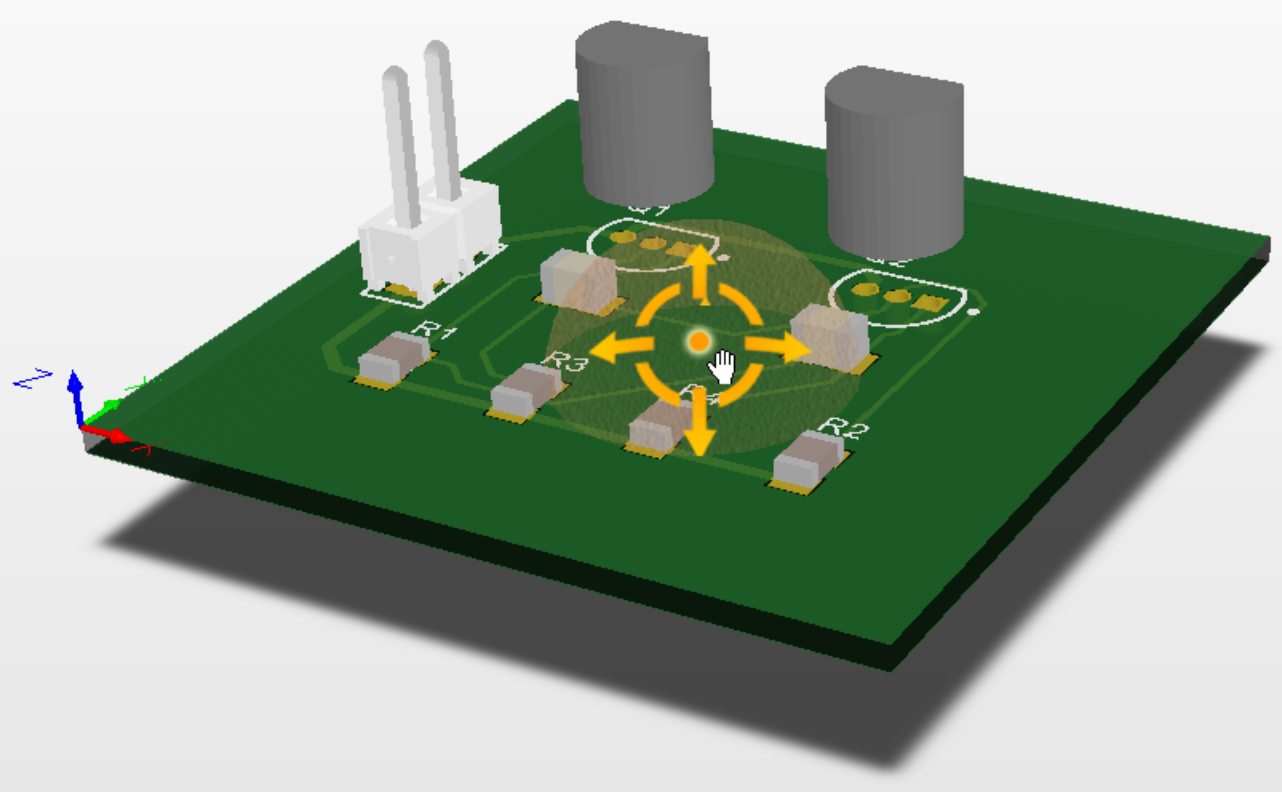
> The PCB editor requires a graphics card that supports DirectX 9.0c and Shader Model 3 (or better).

A powerful feature of Altium Designer is the ability to view your board as a 3 dimensional object. To switch to 3D, run the **View » 3D Layout Mode** command , or press the **3** shortcut. The board will display as a 3 dimensional object - the tutorial board is shown below.

You can fluidly zoom the view, rotate it and even travel inside the board using the following controls:

- **Zooming** - **Ctrl + Right-drag** mouse, or **Ctrl + Roll mouse-wheel**, or the **PgUp** / **PgDn** keys.
- **Panning** - **Right-drag** mouse, or the standard Windows mouse-wheel controls.
- **Rotation** - **Shift + Right-drag mouse**. Note how when you press **Shift** a directional sphere appears at the current cursor position, as shown in the image below. Rotational movement of the model is made about the center of the sphere (position the cursor before pressing Shift to position the sphere) using the following controls. Move the mouse around to highlight and select each one:

- Right-drag sphere when the **Center Dot** is highlighted - rotate in any direction.
- Right-drag sphere when the **Horizontal Arrow** is highlighted - rotate the view about the Y-axis.
- Right-drag sphere when the **Vertical Arrow** is highlighted - rotate the view about the X-axis.
- Right-drag sphere when the **Circle Segment** is highlighted - rotate the view about the Z-plane.



Hold Shift to display the 3D view directional sphere, then click and drag the right-mouse button to rotate.

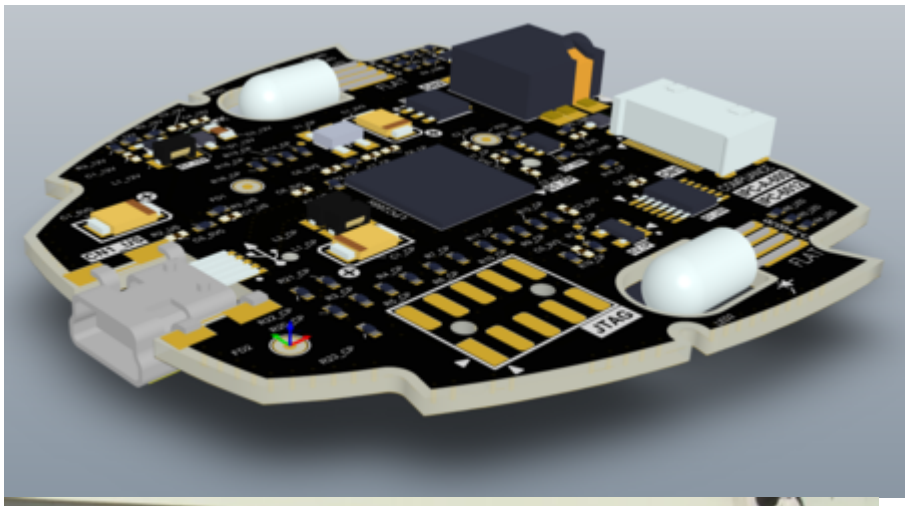
Tips for Working in 3D

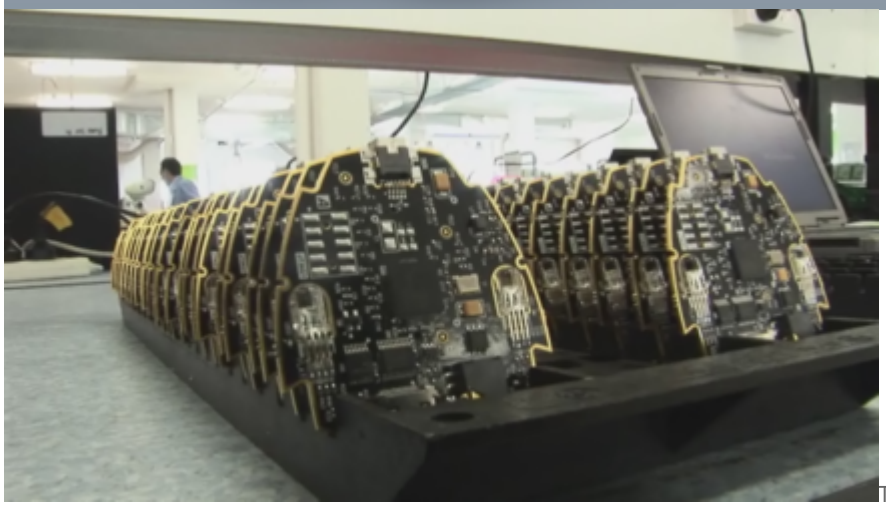
- Press **L** to open the *View Configurations* dialog when the board is in **3D Layout Mode**, where you can configure the 3D workspace display options. There are options to choose various surface and workspace colors, as well as vertical scaling, which is handy for examining the PCB internally. Some surfaces have an opacity setting - the greater the opacity, the less 'light' passes through the surface, which makes objects behind less visible. You can also choose to show 3D bodies or render 3D objects in their (2D) layer color.
- To display the components in 3D, each component needs to have a suitable 3D model.
- You can import a 3D STEP-format model into the component footprint in the Library editor - place a 3D Body Object then select the Generic STEP Model type to embed a STEP model inside that 3D Body Object.
- Check out 3D Content Central for STEP-format component models.
- If there is no suitable STEP model available, create your own component shape by placing multiple 3D Body Objects in the footprint in the Library editor.

If you plan on using the 3D mode regularly then you might like to check out a 3D mouse, such as the Space Navigator from 3Dconnexion, which greatly simplifies the process of moving and rotating the board in 3D layout mode.

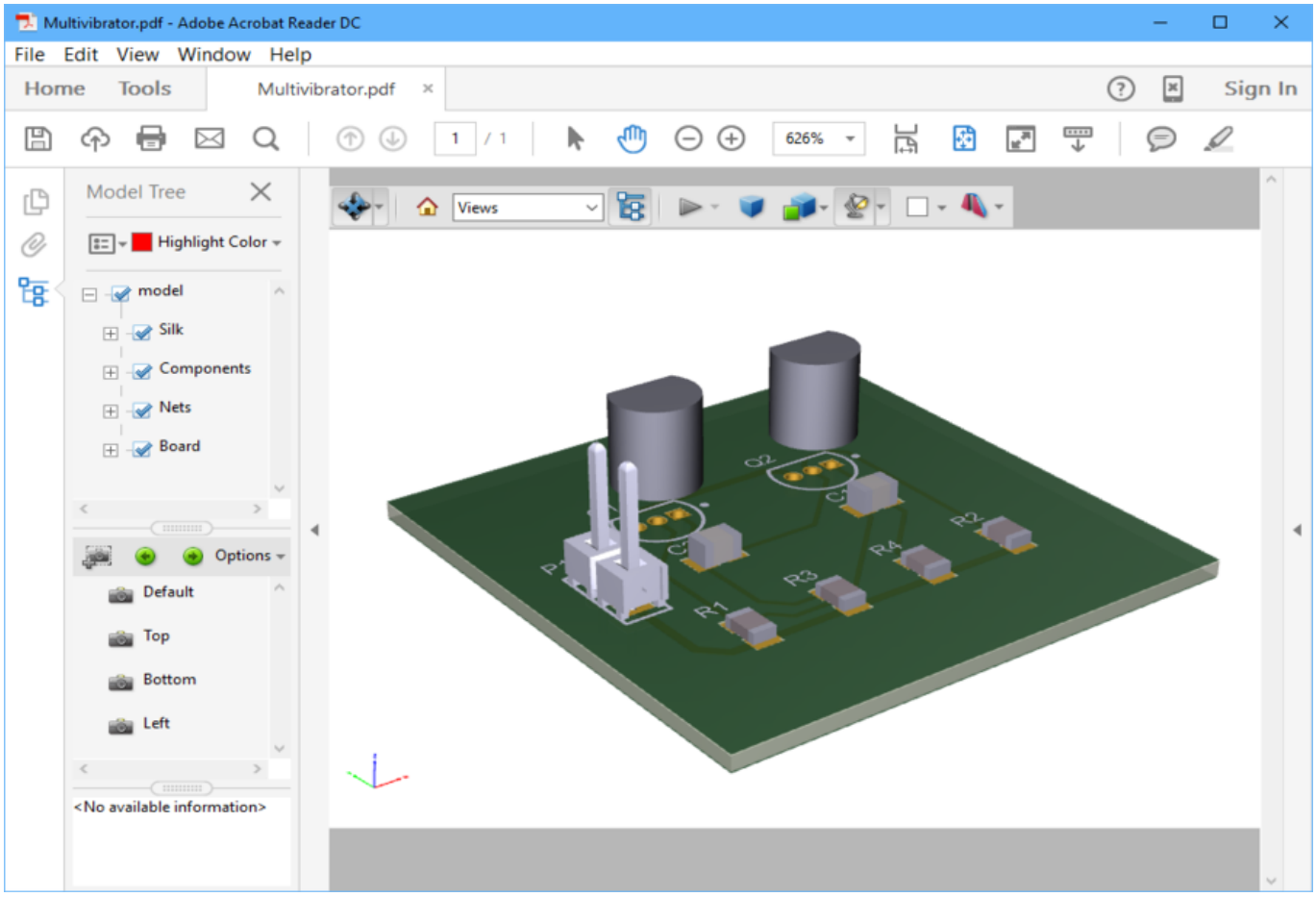
Output Documentation

Now that you've completed the design and layout of the PCB, you're ready to produce the output documentation needed to get the board reviewed, fabricated and assembled.





The ultimate objective is to fabricate and assemble the board.



Output types include PDF 3D, with full zoom, pan and rotate, and the ability to control the display of nets, components and the silkscreen, in Adobe Acrobat Reader®.

Available Output Types

Because a variety of technologies and methods exist in PCB manufacture, the software has the ability to produce numerous output types for different purposes:

Assembly Outputs

- Assembly Drawings - component positions and orientations for each side of the board.
- Pick and Place Files - used by robotic component placement machinery to place components onto the board. Note that the Report Output can also be used to generate Pick and Place files, and is highly configurable.

Documentation Outputs

- PCB Prints - configure any number or printouts (pages), with any arrangement of layers and display of primitives, use this to create printed outputs such as assembly drawings.
- PCB 3D Prints - views of the board from a three-dimensional view perspective.
- PCB 3D Video - output a simple video of the board, based on a sequence of 3D key-frames defined in the PCB editor's *PCB 3D Movie Editor* panel.
- PDF 3D - generate a 3D PDF view of the board, with full support to zoom, pan and rotate in Adobe Acrobat®. The PDF includes a model tree, giving control over the display of nets, components and the silkscreen.
- Schematic Prints - schematic drawings used in the design.

Fabrication Outputs

- Composite Drill Drawings - drill positions and sizes (using symbols) for the board in one drawing.
- Drill Drawing/Guides - drill positions and sizes (using symbols) for the board in separate drawings.
- Final Artwork Prints - combines various fabrication outputs together as a single printable output.
- Gerber Files - creates manufacturing information in Gerber format.
- Gerber X2 Files - a new standard that encapsulates a high-level of design information, with backward compatibility to the original Gerber format.
- IPC-2581 File - a new standard that encapsulates a high-level of design information within a single file.
- NC Drill Files - creates manufacturing information for use by numerically controlled drilling machines.
- ODB++ - creates manufacturing information in ODB++ database format.
- Power-Plane Prints - creates internal and split plane drawings.
- Solder/Paste Mask Prints - creates solder mask and paste mask drawings.
- Test Point Report - creates test point output for the design in a variety of formats.

Netlist Outputs

- Netlists describe the logical connectivity between components in the design and is useful for transporting to other electronics design applications. A large variety of netlist formats are supported.

Report Outputs

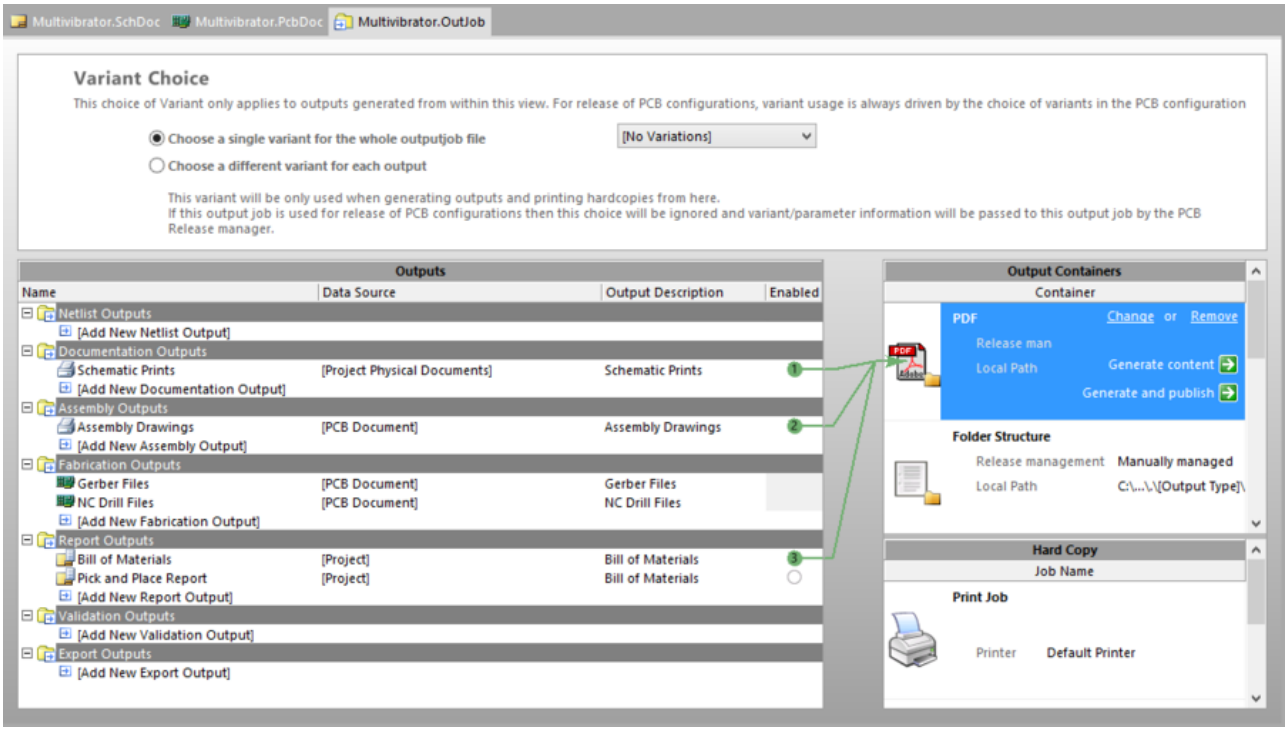
- Bill of Materials - creates a list of parts and quantities (BOM), in various formats, required to manufacture the board.
- Component Cross Reference Report - creates a list of components, based on the schematic drawing in the design.
- Report Project Hierarchy - creates a list of source documents used in the project.
- Report Single Pin Nets- creates a report listing any nets that only have one connection.
- Simple BOM - creates text and CSV (comma separated variables) files of the BOM.
- Electrical Rules Check - formatted report of the results of running an Electrical Rules Check.

Individual Outputs or an Output Job File

Main article: Preparing Multiple Outputs in an OutputJob

Altium Designer has 2 separate mechanisms for configuring and generating output:

1. **Individually** - the settings for each output type are stored in the Project file. You selectively generate that output when required, via the commands in the **Fabrication Outputs**, **Assembly Outputs** and **Export** submenus (accessed from the **File** menu), and the **Reports** menu.
2. **Via an Output Job file** - the settings for each output type are stored in an Output Job file, a dedicated output settings document, which supports all possible output types. These outputs can then be generated manually, or as a managed release.

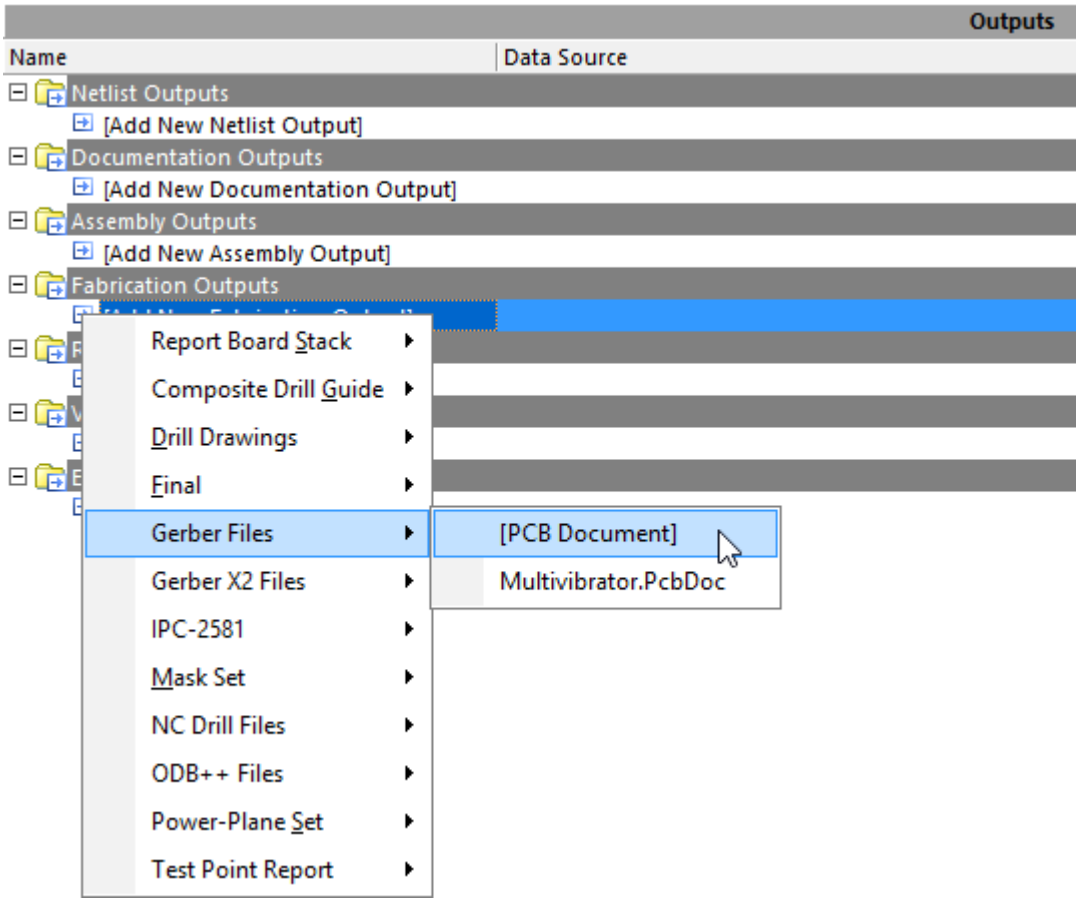


An Output Job file allows you to configure each output type, configure their output naming, format and output location. Output Job files can also be copied from one project to another.

Although the setup dialogs for individual outputs are the same as those used in an Output Job, the settings are independent and must be configured again if you switch from one approach to the other.

Adding an Output Job to the project:

1. In the *Projects* panel, right click on the project name and select **Add New to Project » Output Job File**. A new OutJob will be opened and added to the project.
2. Save the OutJob and name it `Multivibrator`. It will automatically be saved in the same folder as the project file.
3. To add a new Gerber output, click the [Add New Fabrication Output] link in the **Fabrication Outputs** section of the OutJob, and select **Gerber » [PCB Document]**, as shown in the image below. You can select the generic [PCB Document] option if there is only one board in the project, it will automatically be chosen for generation. This also makes the OutJob more easily copied between projects, as this setting will not have to be updated. If there are multiple PCBs in the project you will need to select the specific board.
4. The Gerber output has been added, you will configure it shortly.

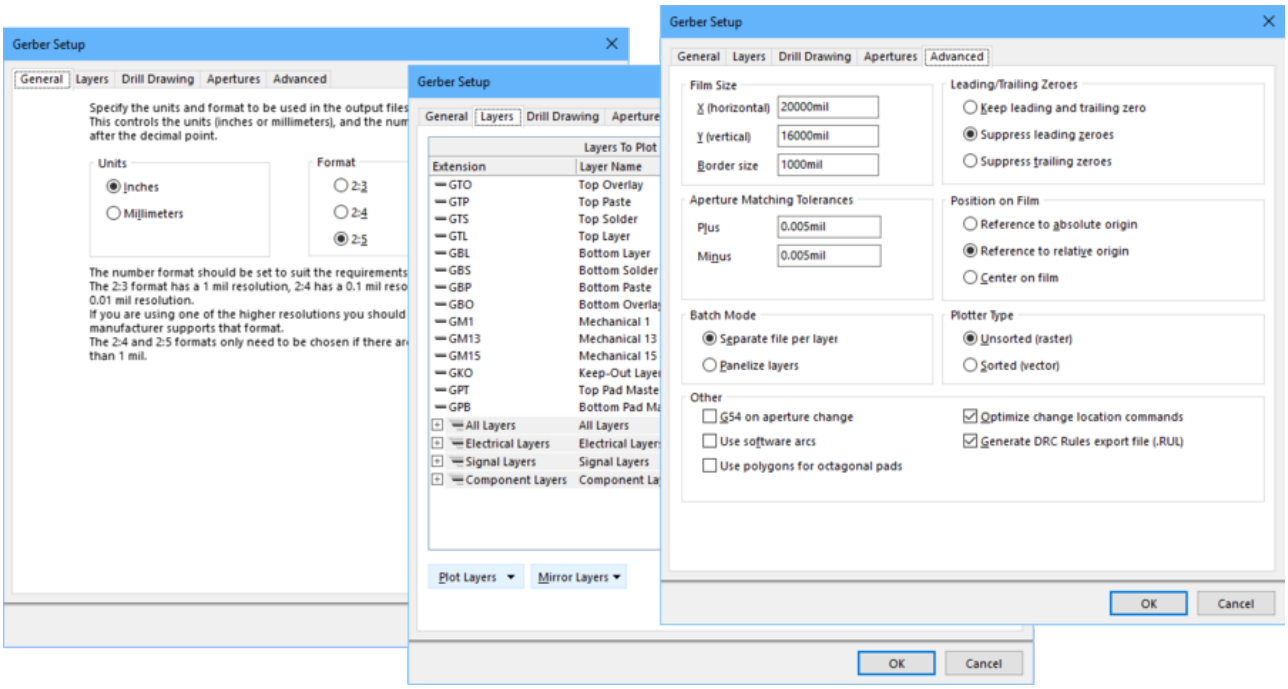


Configuring the Gerber Files

Main article: Gerber Setup

- Gerber continues to be the most common form of data transfer between board design and board fabrication, with ODB++ becoming more and more popular.
- Each Gerber file corresponds to one layer of the physical board - the component overlay, top signal layer, bottom signal layer, top solder mask layer, and so on. It is advisable to consult with your board fabricator to confirm their requirements before supplying the output files required to fabricate your design.
- If the board has any holes then an NC Drill file must also be generated, using the same units, resolution, and position on film settings.
- Gerber files are configured in the *Gerber Setup* dialog, accessed via the PCB Editor's **File »**

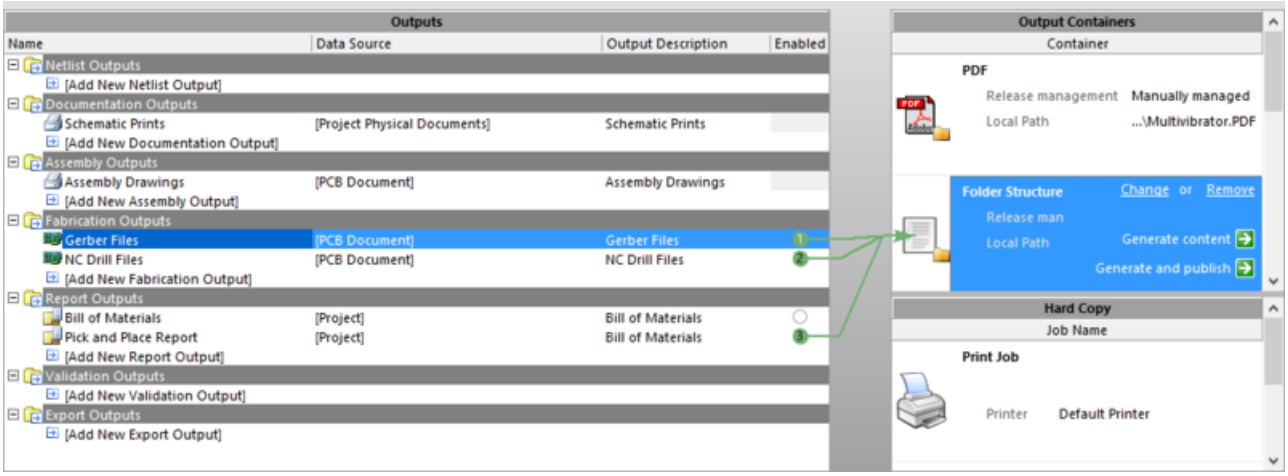
Fabrication Outputs » Gerber Files, or by adding a Gerber output into the **Fabrication Outputs** section of an Output Job, and then double-clicking on it.



Configure the Gerber outputs in the *Gerber Setup* dialog.

[Configuring Gerber generation:]

1. In the OutJob, double-click on the **Gerber Files** output, the *Gerber Setup* dialog will open, as shown in the image above.
2. Since the board has been design in Metric, set the **Units** to **Millimeters**. in the **General** tab of the dialog.
3. The smallest unit used on the board is 0.25mm for the routing and clearance, but because most of the components have their reference point at their geometric center (and were placed on a 1mm grid), some of their pads will actually be on a 0.01 grid. Set the **Format** to **4:3** on the **General** tab, this ensures that the resolution of the output data is more than adequate to cover these grid locations. **Note:** the NC drill file *must always* be configured to use the same **Units** and **Format**.
4. Switch to the **Layers** tab, then click the **Plot Layers** button and select **Used On**. Note that mechanical layers may be enabled, these are not normally Gerbered on their own. Instead they are often included if they hold detail that is required on other layers, for example an alignment location marker that is required on every Gerber file. In this case the **Mechanical Layer** options on the right side of the dialog are used to include that detail with another layer. Disable any mechanical layers that were enabled in the **Layers to Plot** section of the dialog.
5. Click on the **Advanced** tab of the dialog. Confirm that the **Position on Film** option is set to **Reference to relative origin**. **Note:** the NC drill file *must always* be configured to use the same **Position on Film** option.
6. Click **OK** to accept the other default settings and close the *Gerber Setup* dialog.
7. Now the Gerber settings are configured, the next step is to configure their naming and output location. This is done by mapping them to an **Output Container** on the right side of the OutJob. For discrete files with their own file format, you use a Folder Structure container, select **Folder Structure** in the list of Output Containers, then click the radio button for the Gerber Files in the **Enabled** column of the Outputs to map this output to the selected container, as shown below.



The OutJob configured to generate Gerber, NC Drill and Pick and Place output as discrete files.

8. The last step is to configure the Container, to do this click on the **Change** link in the container to open the *Folder Structure Settings* dialog. Across the top are a set of controls which are used to configure if the outputs are Release Managed or Manually Managed, set them to **Manually Managed**. Explore the other options, the lower part of the dialog will display how the names and folder structure changes as you select different options.
9. Click the **Advanced** button at the bottom of the *Folder Structure* dialog and enabled the **Gerber Output** in the list of **CAMtastic Auto-Load Options**. Click **OK** to close the dialog.
10. To generate the Gerber files, click the **Generate Content** link in the **Container** region of the OutJob.
11. The files will be generated and opened in the integrated CAM editor, which can be used for final checking of CAM files before you release them to manufacture. Close the CAM file without saving it.

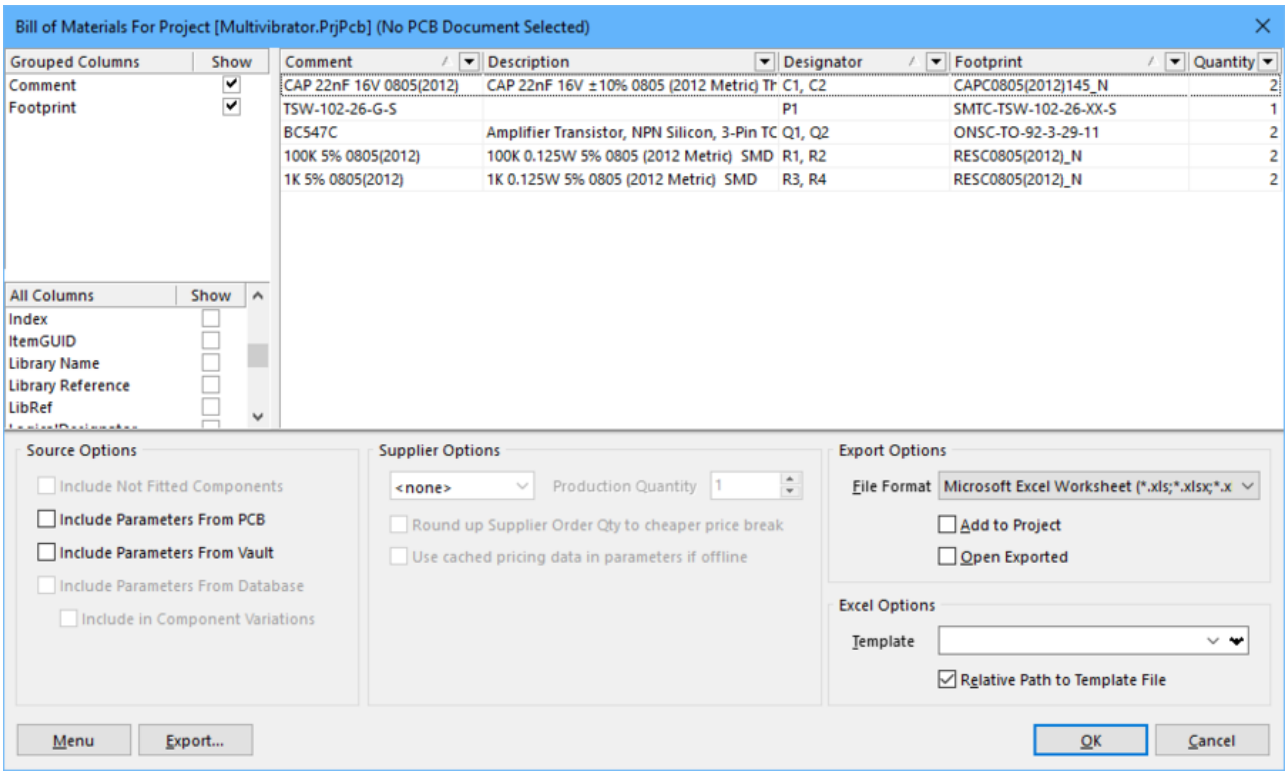
Configuring the Bill of Materials

Main article: Report Manager

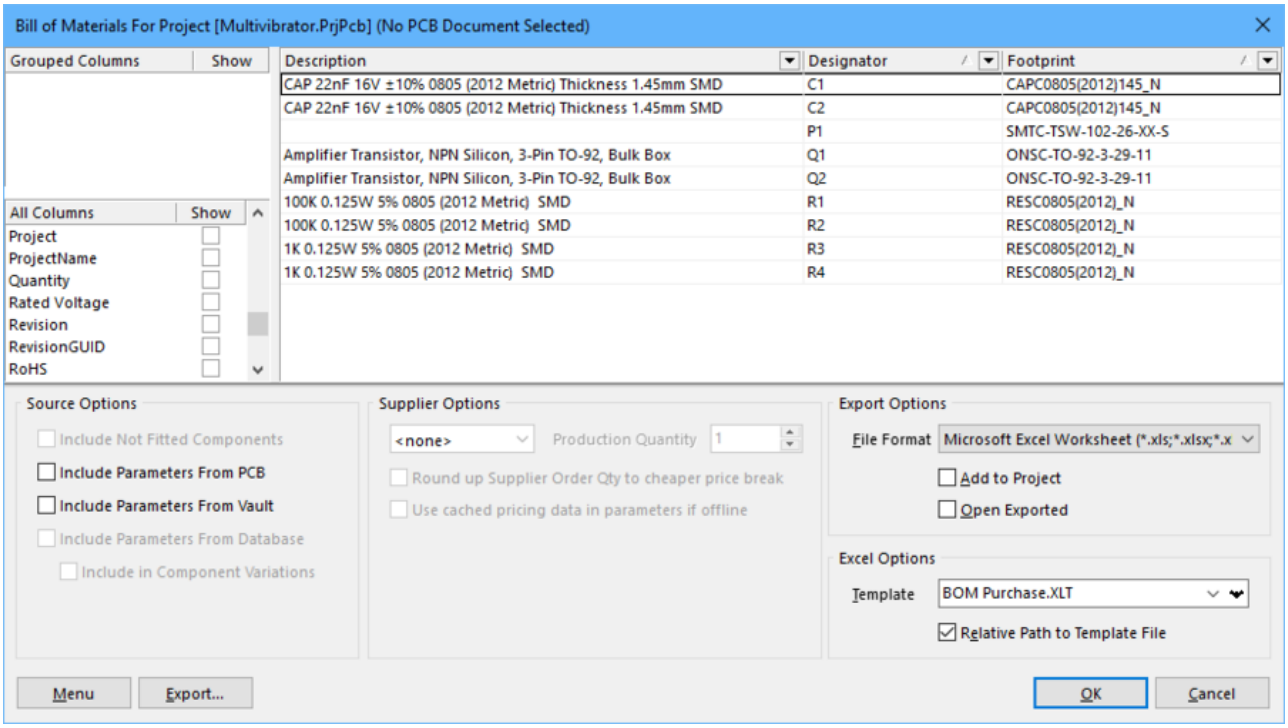
Altium Designer includes a highly configurable BoM generation feature which can generate output in a variety of formats, including: text, CSV, PDF, HTML and Excel. Excel-format BoM's can also have a template applied using one of the pre-defined templates, or one of your own.

- BoM output is configured in the *Bill of Materials For Project* dialog, accessed via the PCB editor's **Reports » Bill of Materials**, or by adding a Bill of Materials into the **Report Outputs** section of an Output Job.
- Down the left of the dialog there is a list of every component attribute, for all components in the design. Enable the checkbox for each attribute you would like to include in the BoM, clear the checkbox for an attribute you wish to remove.
- The default settings for the BoM is to cluster by like components. Clustering is achieved by adding component attributes to the **Grouped Columns** region of the dialog. Click and drag these attributes out of the **Grouped Columns** and drop them back in the **All Columns** region if you prefer every component to be on its own row in the BoM.
- The main grid region of the dialog is the content that is written into the BoM. In this region you can: click and drag to reorder the columns; click on a column heading to sort by that column; ctrl+click to sub-sort by that column; define value-based filters for a column using the small dropdown in each column header; right-click to Force the columns to fit the current dialog width.
- The BoM generator sources its information from the schematic, enable the **Include**

Parameters from PCB option to access PCB information, such as location and side of board (note that this feature can also be used to configure and generate a configurable pick and place file, if required).



The default configuration for a new BoM is to group like components together.



This BoM has been reconfigured to present each component as a unique entry.

Mapping Design Data into the BoM

Design data can be passed from Altium Designer into an Excel Bill Of Materials, by including special statements in the Excel template used to create the BOM.

When creating the Bill of Materials template in Excel, a combination of Fields and Columns can be

used to specify the desired layout. Several example templates are provided with Altium Designer, in the `\Templates` folder of the installation user-files. A list of available fields is detailed below:

Mapping design data into the BoM:

Fields

Fields provide project-level information. These are not usually attached to each item listed in the BOM, but are often used in the header of the document. Fields are used in the format:

Field=FieldName

An example would be **Field=Currency**

The available fields include:

Currency	DataSourceFileName	DataSourceFullPath
GeneratorDescription	GeneratorName	OutputName
OutputType	ProductionQuantity	ProjectFileName
ProjectFullPath	ReportDate	ReportDateTime
ReportTime	TotalQuantity	Title (title of BoM)
VariantName		

Document and Project Parameters

As well as the default Fields listed in the table above, schematic Document Parameters (both default and user-defined in the schematic *Document Options* dialog) and Project Parameters (*Options for PCB Project* dialog) can also be used as Fields.

These are entered as:

Field=ParameterName

If the same parameter exists as both a document parameter and a project parameter, the project parameter takes precedence. If the same document parameter exists in multiple documents, the document parameter that is higher up in the heirarchy takes precedence.

Below are the default document parameters, also referred to as the System parameters.

Address1	Address2	Address3
Address4	ApprovedBy	Author
CheckedBy	CompanyName	ConfigurationParameters
CurrentDate	CurrentTime	Date
DocumentFullPathAndName	DocumentName	DocumentNumber
DrawnBy	Engineer	ImagePath
Index	ModifiedDate	Organization
Revision	Rule	SheetNumber

SheetTotal	Time

Columns

Columns provide the information that is supplied on a per-component basis, and would usually appear on each line in the BOM. Columns are defined by entering the column heading, in the format:

Column=ColumnName

An example would be **Column=Description**, or **Column=LibRef**

Column information can be taken from several sources, including:

- Default component parameters (such as Designator or Description),
- User-defined parameters added to components,
- PCB data,
- Supplier data.

These are discussed separately below.

Default Parameters

These ColumnNames are available for all components:

Comment	ComponentKind	Description
Designator	DesignItemId	Footprint
LibRef	LogicalDesignator	PartType
PhysicalPath	Quantity	UniqueIdName
UniqueIdPath		

PCB Parameters

Pick and Place information can also be included from the PCB. In order to use these columns, the checkbox **Include Parameters From PCB** must be ticked in the BOM Configuration dialog.

Center-X(Mil)	Center-X(mm)	Center-Y(Mil)
Center-Y(mm)	Layer	Pad-X(Mil)
Pad-X(mm)	Pad-Y(Mil)	Pad-Y(mm)
Ref-X(Mil)	Ref-X(mm)	Ref-Y(Mil)
Ref-Y(mm)	Rotation	

Supplier Data

it is possible to retrieve online data from suppliers, and feed that into the BOM. Note that these are updated live, and are retrieved when the BOM is generated. Multiple suppliers can be set up for each component. In the table below, these have been described as *Supplier Info x* - replace x with the appropriate number.

Manufacturer x	Manufacturer Part Number x	Supplier x
Supplier Currency x	Supplier Order Qty x	Supplier Part Number x
Supplier Stock x	Supplier Subtotal x	Supplier Unit Price x

If you have just edited parameters in the schematic and want to see them in the BoM, save the edited documents and recompile the project before generating the BoM.

Explore the sample Excel templates in the `\Altium Designer\Templates` folder. Note that Fields need to be defined above or below the Column region of the template.