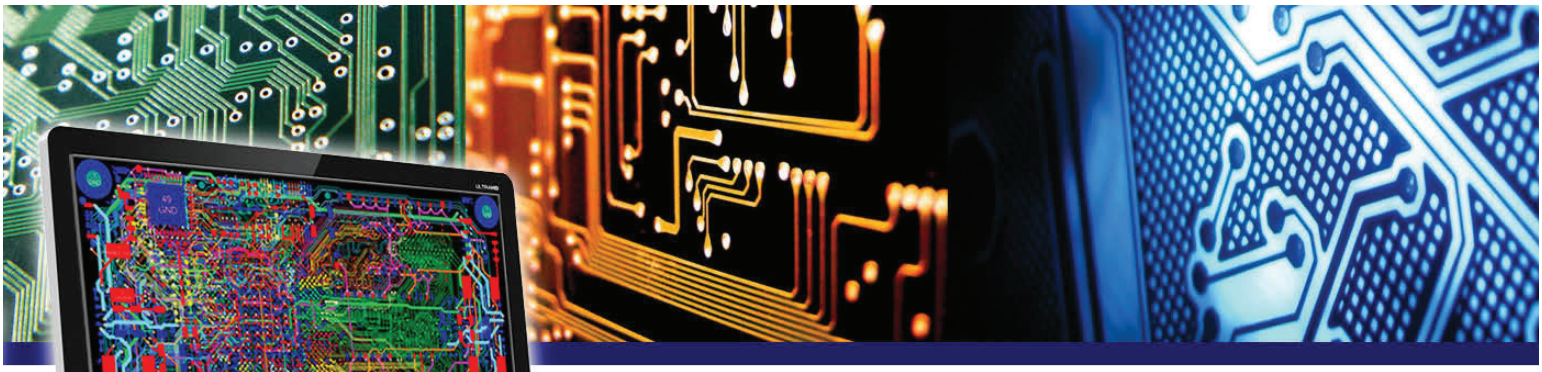

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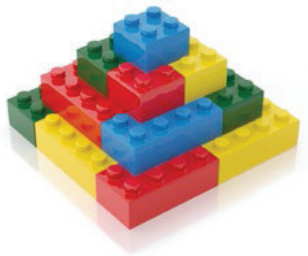
Stackup Planning, Part 1



by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

The PCB substrate that physically supports the components, links them together via high-speed interconnects and also distributes high-current power to the ICs is the most critical component of the electronics assembly. The PCB is so fundamental that we often forget that it is a component and like all components, it must be selected based on specifications in order to achieve the best possible performance of the product. Stackup planning involves careful selection of materials and transmission line parameters to avoid impedance discontinuities, unintentional signal coupling and excessive electromagnetic emissions.

The complexity of electronics design is undoubtedly going to increase in the future, presenting a new set of challenges for PCB designers. Materials used for the fabrication of multilayer PCBs absorb high frequencies and reduce edge rates, thus putting the materials selection process under tighter scrutiny. Ensuring that your board stackup and impedances are correctly configured is a good basis for stable performance.

So where do we start? Over the years, I have found that many engineers and PCB designers do not understand the basic structure that makes up a substrate. We all know that multilayer PCBs consist of signal and plane layers, dielectric material and soldermask coating, but there is a lot more to it.

The most popular dielectric material is FR-4 and may be in the form of core or prepreg (pre-impregnated) material. The core material is thin dielectric (cured fiberglass epoxy resin) with copper foil bonded to one or both sides. For instance: Isola's FR406 materials include 5, 8, 9.5, 14, 18, 21, 28, 35, 39, 47, 59 and 93 mil

ICD Stackup Planner | Field Solver Technology

File Edit Export Import Setup Help

Stackup Planner | PDN Planner

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer | New 8 Layer

UNITS: mil — 9/17/2014 — Total Board Thickness: 63 mil

Differential Pairs > 50/100 | USB | DDR3

Layer No.	Via Span & Hole Diameter			Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadsic Differer
				Soldermask		Liquid Photoimageable	3.8	0.5							
1	8	4	8	Signal	Top	Conductive			2.2	8	4	0.43	53.5	98.11	
				Prepreg		370HR ; 1080 ; Rc= 66% (5GHz)	3.72	2.9							
2				Plane	GND	Conductive			0.7						
				Core		370HR ; 1-1652 ; Rc=43% (5GHz)	4.2	5							
3				Signal	Inner 3	Conductive			0.7	8	4	0.19	54.03	101.32	
				Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8							
4				Plane	VDD	Conductive			0.7						
				Core		370HR ; 3-7628/1080 ; Rc=44% (5G...	4.2	24							
5				Plane	VSS	Conductive			0.7						
				Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8							
6				Signal	Inner 6	Conductive			0.7	8	4	0.19	54.03	101.32	
				Core		370HR ; 1-1652 ; Rc=43% (5GHz)	4.2	5							
7				Plane	GND2	Conductive			0.7						
				Prepreg		370HR ; 1080 ; Rc= 66% (5GHz)	3.72	2.9							
8				Signal	Bottom	Conductive			2.2	8	4	0.43	53.5	98.11	
				Soldermask		Liquid Photoimageable	3.8	0.5							

Design Rule Checker: © 2014 In-Circuit Design Pty Ltd

Figure 1: A typical 8-layer PCB stackup used for high-speed design.

cores. The copper thickness is typically 1/3 to 2 oz. (17 to 70 µm).

The prepreg (B-stage) material is comprised of thin sheets of fiberglass impregnated with uncured epoxy resin which hardens, when heated and pressed, during the PCB fabrication process. Isola's FR406 materials include 1.7, 2.3, 3.9 and 7.1 mil prepregs that may be combined to achieve thicker prepreg.

The most common stackup is called the foil method. This features prepreg with copper foils bonded to the exterior on the outermost layers (top and bottom). Core then alternates with prepreg throughout the substrate. An alternate stackup is known as the capped method, which is the opposite of the foil method and was used by old-school military contractors.

FR-4 has industry approvals of IPC-4101B and is Underwriter Laboratories (UL) recognized for product safety. FR-4 has a glass transition temperature (Tg) of 170°C (the temperature at which the resin begins to flow and the substrate changes to a viscous state) and a decomposition temperature (Td) of 294°C (the temperature at which the substrate breaks down or decomposes). The peak reflow temperature for lead-free solder is 260°C, which is only held for 20 seconds, to reflow solder the surface mount components to the substrate. RF-4 can be used for designs up to 1 GHz.

The Rogers materials (RO4350 & RO4003) are another common dielectric that can withstand higher temperatures (Tg >280°C and Td = 425°C), and they are ideal for high-speed designs up to 10 GHz. But this is somewhat more expensive than FR-4.

The total substrate thickness is generally 62 mil (1.6 mm), but may vary according to the application: 20, 31, 40, 47, 62, 93 and 125 mil are a few other not-so-typical thicknesses. Backplanes, for instance, will typically use the thicker substrate to ensure mechanical support.

One of the steps of the PCB fabrication process is lamination. Core materials are pinned together in a lamination book with sheets of prepreg separating copper layers. The prepreg basically glues the core materials together. Outer layers are made of a foil of copper, which is etched last in the process, so the outer layers of prepreg act as cured core. Horizontal alignment is critical. The stack is pinned between two heavy metal plates and put in a heated hydraulic press for about two hours, until cured.

In Figure 3, the left stackup has a total thickness of 9 mil. However, when the board is cured the resin in the prepreg (green) flows around the signal traces below (as in the right diagram). This envelopes the trace completely, and also thins the prepreg material. As the signal trace becomes closer to the above plane, the impedance drops.

So, here are a few effects of the prepreg being cured:

a) The total board thickness reduces, by the thickness of the signal layer copper, as the trace is totally enveloped in resin from the prepreg. The resin also flows into the antipads of the nearby planes and oozes from the sides of the lamination book.

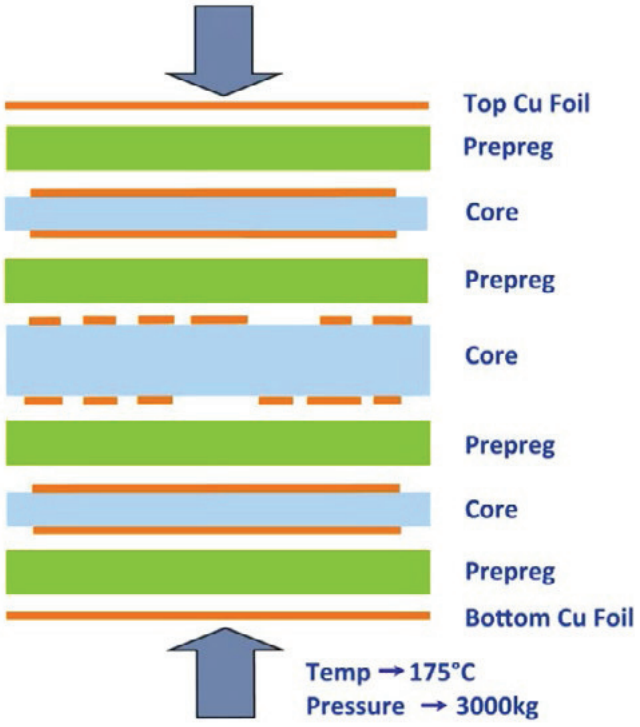


Figure 2: The PCB lamination process.

STACKUP PLANNING, PART 1 *continues*

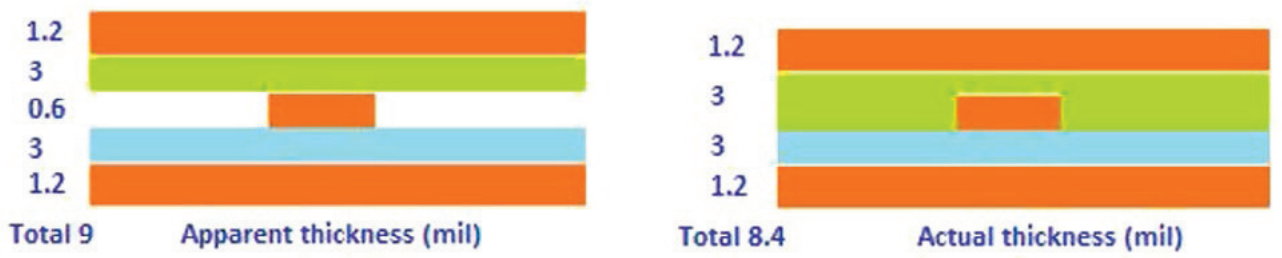


Figure 3: Total board thickness.

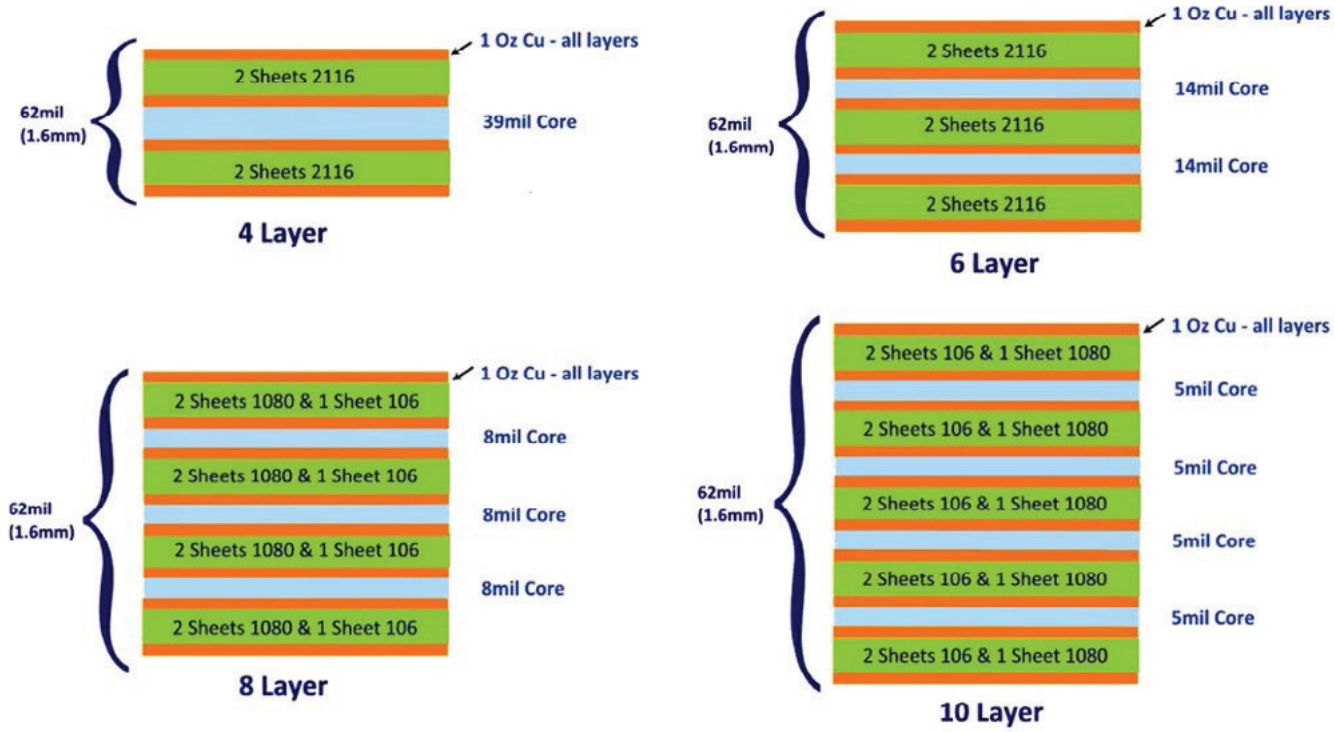


Figure 4: Typical stackups. (source: Advanced Circuits)

b) The impedance of the signal trace reduces as the resin flows out of the prepreg around the traces and makes the prepreg thinner. This results in the trace becoming closer to the plane.

c) The edge of the PCB can have less resin than the centre (and therefore slightly different impedance) due to resin flowing out of the edge of the lamination book. The resin/glass percentage, across the entire panel, determines the impedance—the more resin the higher the impedance.

d) Buildup layers—the outer most prepreg and copper—are etched last in the fabrication process so the resin does not flow around the outer layer copper traces. In this case, the trace thickness is added to the total board thickness and the impedance does not change.

The stackups of Figure 4 are typical stackups for 62 mil substrates, although they may vary between PCB fabricators as they may stock different materials.

Please note the following:

- The outermost dielectric is prepreg.

- The outer prepreg has a copper foil coating.
- Prepreg layers may be combined with (multiple) sheets of prepreg separating them. For instance, two sheets of 1080 and one sheet of 106 prepreg material may be required to achieve the desired thickness.

So where do we start in an attempt to build the perfect stackup for our project? Initially, virtual materials are used to get the rough numbers. Obviously, every digital board will require 50 ohms impedance and generally a 100 ohm differential pair. This is our target impedance. However, multiple technologies are often used on complex designs.

Keep these tips in mind when planning the board stackup:

- All signal layers should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies. Closely coupled planes reduce AC impedance at the top end and dramatically reduce electromagnetic radiation.
- High-speed signals should be routed between the planes to reduce radiation.
- Reducing the dielectric height will result in a large reduction in your crosstalk without having a negative impact on available space on your board.
- The substrate should accommodate a number of different technologies. For example: 50/100 ohm digital, 40/80 ohm DDR4, 90 ohm USB.

Unfortunately, not all of these rules can be accommodated on a four-layer or six-layer board simply because we have to use a buffer core in the center to realize the total board thickness of 62 mil. However, as the layer count increases, these rules become more critical and should be adhered to.

Part 2 of the Stackup Planning series will continue detailing the construction of typical, high layer-count stackups and build-up technology.

Points to Remember

- The PCB substrate is the most critical component of the electronics assembly.
- Ensuring that your board stackup and impedances are correctly configured is a good basis for stable performance.
- Dielectric material may be in the form of core or prepreg (pre-impregnated) material. The core material is thin dielectric (cured fiberglass epoxy resin) with copper foil bonded to one or both sides. The prepreg material is thin sheets of fiberglass impregnated with uncured epoxy resin which hardens when heated and pressed.
- The total substrate thickness is generally 62 mil (1.6 mm) but may vary according to the application.
- When the board is cured, the resin in the prepreg flows around the signal traces below, thus enveloping the trace completely and also thinning the prepreg material. This alters the impedance of the signal traces.
- To construct a stackup: Initially, virtual materials are used to get the rough numbers then exact materials from the library are introduced to improve accuracy. **PCBDESIGN**

References

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2. Henry Ott: Electromagnetic Compatibility Engineering.

3. Bob Tarzwell: Controlled Impedance.

4. The ICD Stackup and PDN Planner: www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.