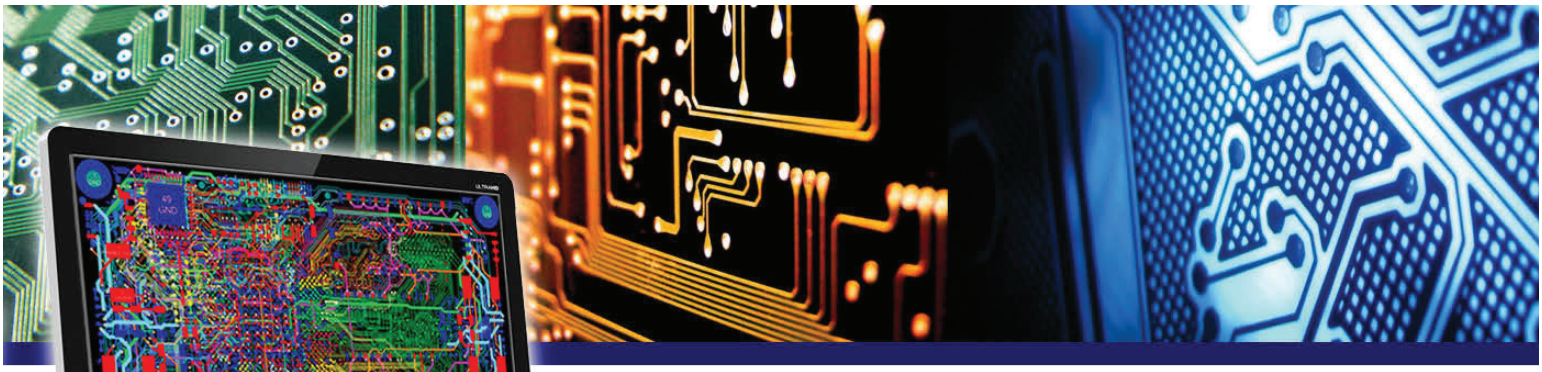

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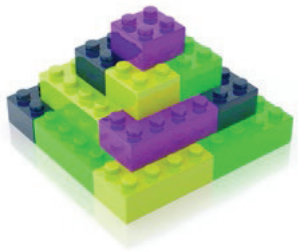
Stackup Planning, Part 3



by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Following on from the first Stackup Planning columns, this month's Part 3 will look at higher layer-count stackups. The four- and six-layer configurations are not the best choice for high-speed design. In particular, each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk. As the layer count increases, these rules become easier to implement but decisions regarding return current paths become more challenging.

Given the luxury of more layers:

- Electromagnetic compliancy (EMC) can be improved or more routing layers can be added.
- Power and ground planes can be closely coupled to add planar capacitance, which is essential for GHz plus design.
- The power distribution networks (PDNs) can be improved by substituting embedded capacitance material (ECM) for the planes.
- Multiple power planes/pours can be defined to accommodate the high number of supplies required by today's processors and FPGAs.
- Multiple ground planes can be inserted to reduce the plane impedance and loop area.

Although power planes can be used as reference planes, ground is more effective because local stitching vias can be used for the return current transitions, rather than stitching decoupling capacitors which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But, if one sticks to the basic rules, then the best performing configurations are obvious.

Figure 1 illustrates the spreading of return current density across the plane above and below the signal path. At high frequencies, the return current takes the path of least inductance. As the frequency approaches a couple of hundred MHz, the skin effect forces the return current to the surface (closest to the signal trace).

I previously mentioned that it is important to have a clearly defined current return path. But it is also important to know exactly where the return current will flow. This is particularly critical with asymmetric stripline configurations where one signal layer is sandwiched between two planes as in Figure 2. Now obviously, if the distance to the closest plane (h1) is the same distance as the far plane (h2) then the return current distribution will be equal on each plane (given the same inductance for each path). However, in order to force the current onto the ground (GND) plane of an unbalanced stripline configuration, h2 needs to be at least twice h1, and three times is better.

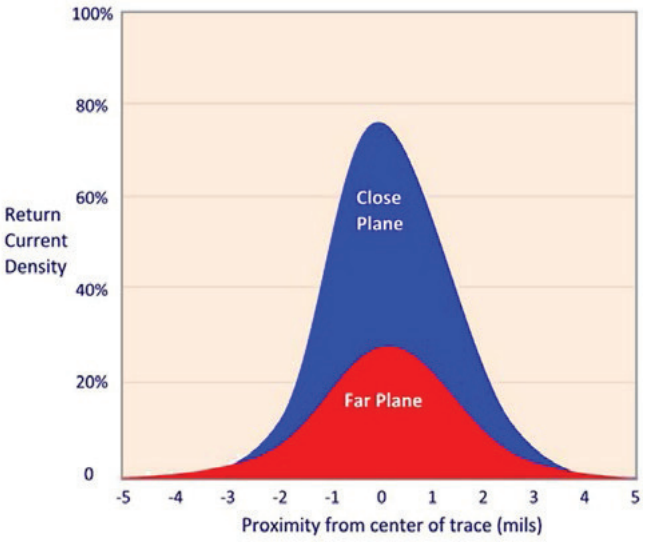


Figure 1: Return current density for asymmetric stripline planes of ratio 3:1.

STACKUP PLANNING, PART 3 *continues*

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
1	8	Plane	GND	Conductive			1.4					
		Core		Dielectric	4.3	5	Close plane (h1)					
2		Signal	Inner 3	Conductive			1.4	12	4	0.31	54.2	102.11
		Prepreg		Dielectric	4.3	15	Far plane (h2)					
3		Plane	Power	Conductive			1.4					

Figure 2: Close plane is h1 (5 mils), far plane is h2 (15 mils).

$$Iclose = \left(1 - \frac{h1}{h1 + h2}\right).I \quad \text{Equation 1}$$

$$Ifar = \left(\frac{h1}{h1 + h2}\right).I \quad \text{Equation 2}$$

Equations 1 and 2 define the relationship between the ratio of the thicknesses of the dielectrics to the close and far planes and the resultant return current distribution. Table 1 simplifies the calculations presenting the percentage of return current, in each plane, for different ratios of h2:h1. If the configuration is dual asymmetric stripline (two signal layers between the planes), then these ratios still apply and can be calculated by adding the two (or more) dielectric thicknesses to the far plane representing the h2 value.

Ratio h2:h1	Close Plane	Far Plane
1:1	50%	50%
2:1	67%	33%
3:1	75%	25%
4:1	80%	20%
5:1	83%	17%
6:1	86%	14%
7:1	88%	12%
8:1	89%	11%
9:1	90%	10%
10:1	91%	9%

Table 1: Percentage of return current in the close and far planes of asymmetric striplines.

Eight-Layer Stackup

An eight-layer board with six routing layers is not recommended. If six routing layers are required, then a 10-layer board should be used. For that reason, an eight-layer board can be thought of as a six-layer board with optimum EMC performance and should not be utilized to improve routability. Although there are many possible configurations of eight layers, I will only focus on the two that I consider to possess superior performance. Having said that, there are a total of four signal layers and four plane layers to consider in the each configuration.

1. The stackup of Figure 3 is the standard eight-layer configuration. This stackup has many good attributes including:

- All signal layers are adjacent to, and closely coupled to, an uninterrupted reference GND plane, which creates a clear return path and eliminates broadside crosstalk.
- Stripline return current is biased toward the GND planes.
- There is good planar capacitance (4 mils VDD to GND spacing) to reduce AC impedance at high frequencies.
- ECM could also be substituted for the center planes, further improving the PDN performance.
- Crosstalk is minimized by closely coupling the signal to plane layers.
- EMI is minimized by routing critical signals between the planes.
- The substrate can accommodate a number of different technologies. For example: 50/100 ohm digital and 90 ohm USB.

Differential Pairs > 50/100 ohms USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Dielectric	3.3	0.5						
1	8	Signal	Top	Conductive			2.0	10	4	0.4	51.61	97.17
		Prepreg		Dielectric	4.3	3						
2		Plane	GND	Conductive			1.4					
		Core		Dielectric	4.3	5						
3		Signal	Inner 3	Conductive			1.4	10	4	0.31	54.16	99.48
		Prepreg		Dielectric	4.3	15						
4		Plane	VDD	Conductive			1.4					
		Core		Dielectric	4.3	4						
5		Plane	GND	Conductive			1.4					
		Prepreg		Dielectric	4.3	15						
6		Signal	Inner 6	Conductive			1.4	10	4	0.31	54.16	99.48
		Core		Dielectric	4.3	5						
7		Plane	GND	Conductive			1.4					
		Prepreg		Dielectric	4.3	3						
8		Signal	Bottom	Conductive			2.0	10	4	0.4	51.61	97.17
		Soldermask		Dielectric	3.3	0.5						

Figure 3: Standard eight-layer stackup with central planar capacitance using virtual materials.

Differential Pairs > 50/100 ohms USB 90 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5						
1	8	Signal	Top	Conductive			2.0	12	4	0.4	51.42	98.53
		Prepreg		IT-180A; 1080; Rc=62%; (2GHz)	3.9	2.8						
2		Plane	GND	Conductive			1.4					
		Core		IT-180A; 1-2116; (2GHz)	3.8	4						
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	52.2	99.69
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
4		Plane	SPLIT POWER	Conductive			1.4					
		Core		Dielectric	4.3	4						
5		Plane	SPILT POWER	Conductive			1.4					
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
		Prepreg		IT-180A; 7628; Rc=43%; (2GHz)	4.0	7.4						
6		Signal	Inner 6	Conductive			1.4	12	4	0.31	52.2	99.69
		Core		IT-180A; 1-2116; (2GHz)	3.8	4						
7		Plane	GND	Conductive			1.4					
		Prepreg		IT-180A; 1080; Rc=62%; (2GHz)	3.9	2.8						
8		Signal	Bottom	Conductive			2.0	12	4	0.4	51.42	98.53
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5						

Figure 4: Alternate eight-layer stackup with central split power planes using ITEC IT-180A 2GHz material.

Probably the only negative, for this configuration, is that it will not accommodate multiple power supplies on the lone power plane. Today's high-speed processors and FPGAs require more than six or seven different high current power sources. So if you are pushing the envelope then this configuration is probably not right for you. A recent complex layout that I completed had a total of 13 individual power supplies. As this is becoming the norm, additional power planes need to be exploited and these need to be split to accommodate all 13 supplies plus GND.

2. The alternate configuration of Figure 5 alleviates the multiple power supply issue but does this by sacrificing planar capacitance. So in order to compensate, for this shortcoming, the PDNs need to have multiple decoupling capacitors with self-resonances close to the fundamental clock frequency. Also, lower mounting inductance can be achieved by placing these decaps on the top layer so that the fanout vias connect to planes 2 and 5 rather than transverse the total layer span. This also helps lower the high-frequency AC impedance.

STACKUP PLANNING, PART 3 *continues*

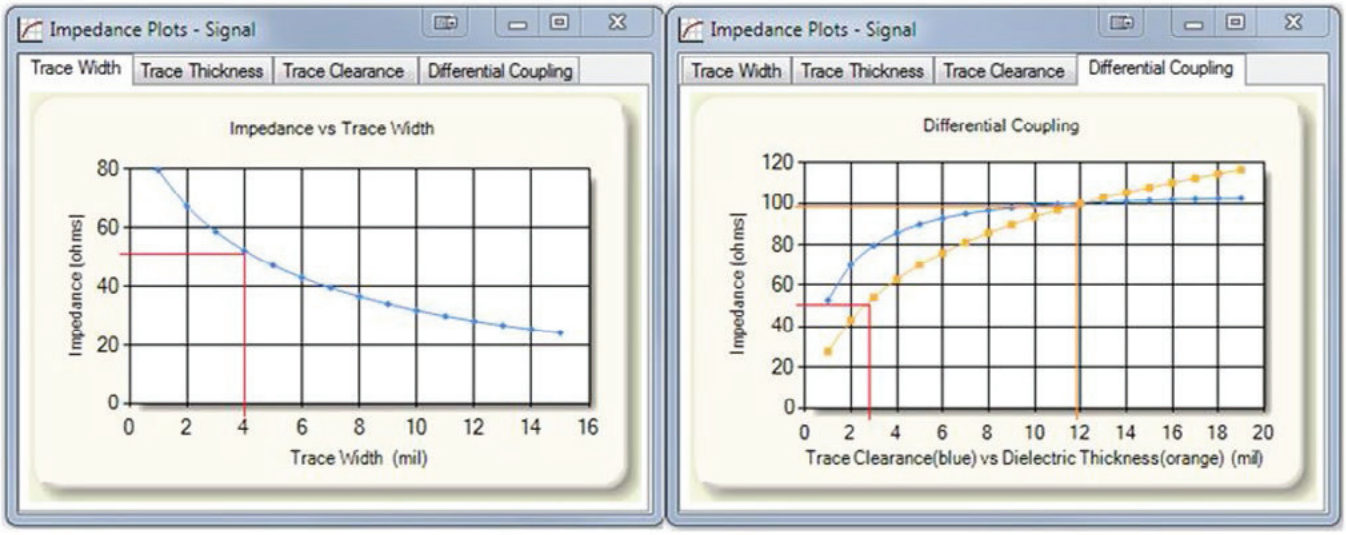


Figure 5: Impedance plots for the microstrip layers.

I have mentioned in previous columns that planes should not be split. This mainly refers to having one continuous GND plane for all supplies including analog. But since, in this case, the return current path has been forced into the GND planes then the path is not interrupted. Looking at the asymmetric stripling configuration between layers 2 and 4 of Figure 4, we have a ratio of 14.8:4. This means that at least 79% of this current will flow in the GND plane. However, if you also take into account the increased inductance, of the alternate return path, this almost totally eliminates the power plane. It is important to place GND stitching vias close to each signal layer transition to ensure there is a low inductance path between GND planes.

Figure 5 incorporates ITEC IT-180A 2GHz materials. This material is very common in Asia and is suitable for low-cost, high-speed applications. It has a low dielectric constant and low dielectric loss of just 0.015 with a glass transition temperature of 180C. Since the "real" values are quite different to the "virtual" values, I have used to initially construct the stackup, the variables must be adjusted to provide the correct impedances for the design.

The impedance plots of Figure 5, project the correct values of trace width (4 mils), trace thickness (2 mils), trace clearance (12 mils) and dielectric thickness (2.8 mils) given the dielectric constant (3.9) for the ITEC IT-180A 2GHz material to achieve the target single ended and differential impedance. This also provides the differential coupling point whereby increasing the trace spacing has little effect as the impedance rolls off. In this case, 12 mils is ideal for 100 ohms differential impedance.

Next month, Part 4 of the Stackup Planning series will continue detailing the construction of 10+ stackup layer configurations. Once the basics are defined, the pattern for higher layer-count structures becomes evident.

Points to Remember

- Each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- Although power planes can be used as reference planes, ground is more effective.
- At high frequencies, the return current takes the path of least inductance.
- In order to force the current onto the ground (GND) plane of an unbalanced stripline configuration, h2 needs to be at least twice h1; three times is even better.
- An eight-layer board can be thought of as a six-layer board with optimum EMC performance and should not be utilized to improve routability.

- Additional power planes need to be exploited and these need to be split to accommodate all supplies plus GND.
- The impedance plots project the correct values of all variables for the chosen material to achieve the target impedance. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Material Selection for SERDES Design, Material Selection for Digital Design, The Perfect Stack-up for High-Speed Design, and Embedded Signal Routing.

2. Henry Ott: Electromagnetic Compatibility Engineering.

3. To download the ICD Stackup and PDN Planner, visit www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.

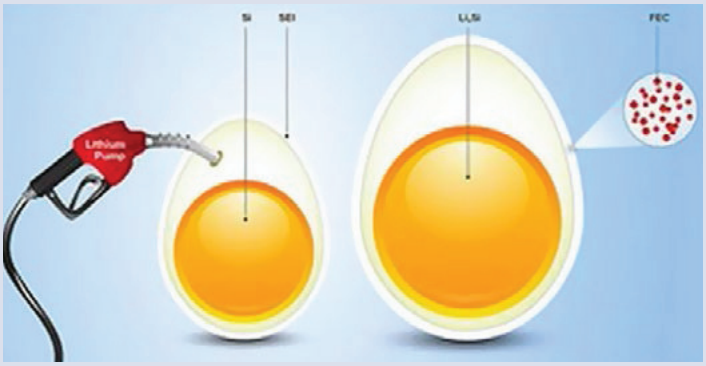
Protective Shells May Boost Silicon Lithium-ion Batteries

Imagine a cell phone that charges in less than an hour and lasts for three to four days, or an electric car that runs for hundreds of miles before needing to be plugged in.

Researchers at the U.S. Department of Energy's Argonne National Laboratory are working to make this dream a reality by developing lithium-ion batteries containing silicon-based materials. The most commonly used commercial lithium-ion batteries are graphite-based, but scientists are becoming increasingly interested in silicon because it can store roughly 10 times more lithium than graphite.

There's just one problem: current batteries based on silicon materials don't last long.

The problem lies in the battery's chemistry. The electrolyte inside the battery transports lithium ions back and forth between positive and negative electrodes as the battery charges and discharges.



Lithium ions react with the negative electrode to form a new compound, causing the electrode to expand, while the electrolyte produces a protective coating called the solid electrolyte interphase.

"The ideal solid electrolyte interphase should halt the reaction between the electrode and electrolyte, while allowing the lithium to come through," said Ilya Shkrob, a chemist in the Chemical Sciences and Engineering Division.

But the coating also needs to expand and contract with the electrode, or else it will crack and the battery won't work.

"When the protective layer cracks, the electrode surface reacts and consumes the electrolyte," Shkrob said. "If the electrolyte is completely consumed, then the battery won't work."

In today's graphite-based lithium-ion batteries, the electrode expands about 10%—a small enough change that cracks in the coating aren't an issue.

But the electrode in a silicon-based lithium-ion battery expands up to 300%. These batteries need a different electrolyte in order to produce an elastic shell.

The researchers found that when fluorine is added to ethylene carbonate, the resulting electrolyte forms a coating that can stretch and accommodate the volume changes in the electrode.