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Stackup Planning, Part 4

by Barry Olney
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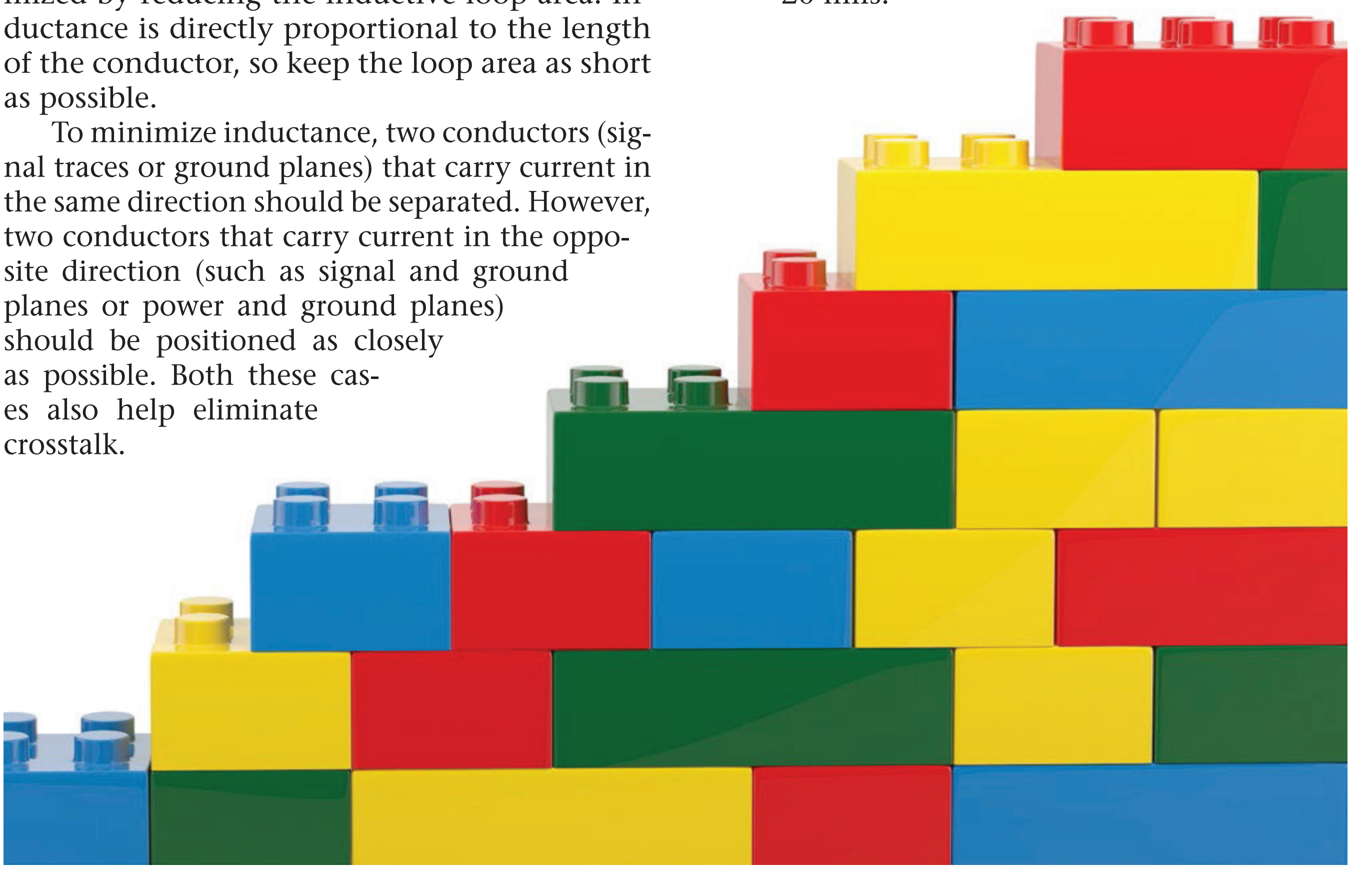
In the final part of the Stackup Planning series, I will look at 10-plus layer counts. The methodology I have set out in previous columns can be used to construct higher layer-count boards. In general, these boards contain more planes and therefore the issues associated with split power planes can usually be avoided. Also, 10-plus layers require very thin dielectrics, in order to reduce the total board thickness. This naturally provides tight coupling between adjacent signal and plane layers reducing crosstalk and electromagnetic emissions.

In high-speed digital designs, transient ground currents are the primary source of both unwanted noise voltages and radiated emissions. In order to minimize these emissions, the impedance of the ground should be minimized by reducing the inductive loop area. Inductance is directly proportional to the length of the conductor, so keep the loop area as short as possible.

To minimize inductance, two conductors (signal traces or ground planes) that carry current in the same direction should be separated. However, two conductors that carry current in the opposite direction (such as signal and ground planes or power and ground planes) should be positioned as closely as possible. Both these cases also help eliminate crosstalk.

Here are some additional rules for high-speed design:

1. Use multiple ground planes, where possible, rather than power planes, in the stackup to isolate signal layers.
2. Place stitching ground vias close to every signal transition (via) to provide a short current return path.
3. Spread numerous ground stitching vias around the board to connect the multiple ground planes through a low impedance path.
4. Don't use ground pours on signal layers as this reduces the impedance of nearby traces. If you must, in order to balance copper, separate the signal and pour by 20 mils.



If power planes are used as reference planes, then the return current must transverse stitching capacitors in order to jump between ground and power planes. The current flowing through these stitching capacitors will create a voltage drop across them. These voltages may radiate adding to system noise problems.

Determining the required layer count: the number one question!

Over the years, a number of people have put forward equations to determine the route density. Rent's Rule is one such model.

$$Trace\ Pitch = \frac{\sqrt{X.Y}}{n}\ 2.7M$$

where: n is the number of nets
X and Y are the board width and length in inches
M is the number of routing layers

Good luck getting any serious results from such equations. There are just too many variables to take such a basic approach to layer count determination. This is my line of attack:

As with Rent's Rule, I start with the route pitch. Technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable whilst minimizing PCB fabrication costs. Technology of 4/4 mil (trace/clearance) and vias of 18/8 mil (pad/hole) are generally required for complex high-speed designs incorporating BGAs. However, if you can use less demanding dimensions, then this will reduce cost and improve fabrication yield.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50/100 ohm Zo/Zdiff are used. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN). While higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of Zo, for a digital design, is 50–60 ohms.

The total number of layers required for a given design is dependent on the complexity of the design. Factors include:

- The number of signal nets that must break out from a BGA.
- The number of power supplies required by the BGAs.

Differential Pairs > 50/100 Digital | 40/80 DDR3 | 90 USB

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5							
1	8 4 4	Signal	Top Layer	Conductive			1.38	10	4.5	0.34	52.11	99.44	
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63							
2		Plane	GND_TOP	Conductive			1.38						
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
3		Signal	MidLayer3	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
4		Signal	MidLayer4	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
5		Plane	GND	Conductive			1.38						
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
6		Plane	PWR	Conductive			1.38						
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
7		Signal	MidLayer7	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
		Prepreg		N4000-13; 3313; Rc=58% (2.5GHz)	3.50	4.32							
		Prepreg		N4000-13; 2116; Rc=55% (2.5GHz)	3.56	5.58							
8		Signal	MidLayer8	Conductive			1.38	12	4	0.31	52.16	98.69	95.35
		Core		N4000-13; 1080; Rc=61.2% (2.5GHz)	3.4	3							
9		Plane	GND_BOT	Conductive			1.38						
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63							
10		Signal	Bottom Layer	Conductive			1.38	10	4.5	0.34	52.11	99.44	
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI (1GHz)	3.5	0.5							

Figure 1: A 10-layer configuration using Nelco N4000-13 2.5GHz material.

- The component density and package types.
- If there are BGAs of 0.8 mm or less, plated-through-hole (PTH) vias will impede the routing.
- Also, with high layer count boards, the via aspect ratio will increase the diameter of the vias. Via length to hole aspect ratio should be less than 8:1 or the reliability will decline significantly. In this case, a combination of PTH and blind and buried vias may be required.

Experienced PCB designers get a feel for it after a while, but a good way to check if you have enough layers is to autoroute the board. With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable. The performance of the autorouter also impacts on the completion rate. You may have to re-evaluate the placement a couple of times to get the best results. In general, eight layers is a good starting point for DDR type designs. Remember, it is much easier to increase the number of layers than to reduce them, so start with the minimum.

10-Layer Stackup

A 10-layer board is similar to an eight-layer with the addition of two more embedded signal layers.

These are used to increase routability and to add planar capacitance. I have used Nelco N4000-13 2.5GHz material (Figure 1). This is another common high-speed material. The stackup accommodates 50/100 ohm digital, 40/80 ohm DDR3 and 90 ohm USB. Also, I have a combination of PTH and blind and buried vias with appropriate aspect ratios for a total board thickness of 60.82 mils. In this case, internal layers 3, 4, 7 and 8 can be used for the DDR3 routing as three of these layers are referenced to GND whilst the other (layer 7) is referenced to the 1.5V DDR3 PDN (or 1.35V in the case of lower power devices). The layer 7 power plane can have a 1.5V island directly above the DDR3 devices. With a 4.32 mil dielectric between the planes, there is also excellent planar capacitance of about 240 pF/in^2. This will reduce the AC impedance of the DDR3 PDN at frequencies about 1GHz which is required for this type of design.

The outer microstrip layers should not be used for routing—except for fanout. Apart from the fact that outer layers radiate more than internal layers, they also vary considerably in impedance. This is due the uneven plating thickness of the final electrolysis process used to plate the though-hole barrels during fabrication. Blind vias can be used to fanout from the BGA and drop directly to either GND or layer 3. The PTH could be used to transverse the signals to the other layers or alternatively a buried via could be used.

Figure 2 illustrates an alternative of buildup microstrip (outer layers). In this case, layer 1 is only used for fanout to layer 2, GND or Power. But layer 2 can be used for high-speed routing of SERDES or other differential signals. It is closely coupled to the layer 3 (GND plane) and will have constant impedance.

12-Plus Layout Count

I could go on and describe each successive layer count in detail, but I'm sure you get the drift by now. Figure 3 illustrates the signal/plane configuration for 12–18 layers. There are of course, many variations that could be employed depending on the application. The ICD Stackup Planner has default stackups from 2–18

Layer No.	Via Span & Hole Diameter			Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
				Soldermask		Dielectric	3.3	0.7						
1	8	4	8	Signal	Top	Conductive			2.2	10	5.5	0.55	70.13	121.81
				Prepreg		Dielectric	3.7	3.4						
2				Signal	Inner 2	Conductive			0.6	10	4.5	0.18	53.5	99.23
				Core		Dielectric	3.6	3						
3				Plane	GND	Conductive			0.6					
				Prepreg		Dielectric	3.5	3						
4				Plane	VDD	Conductive			0.6					

Figure 2: Buildup microstrip layers.

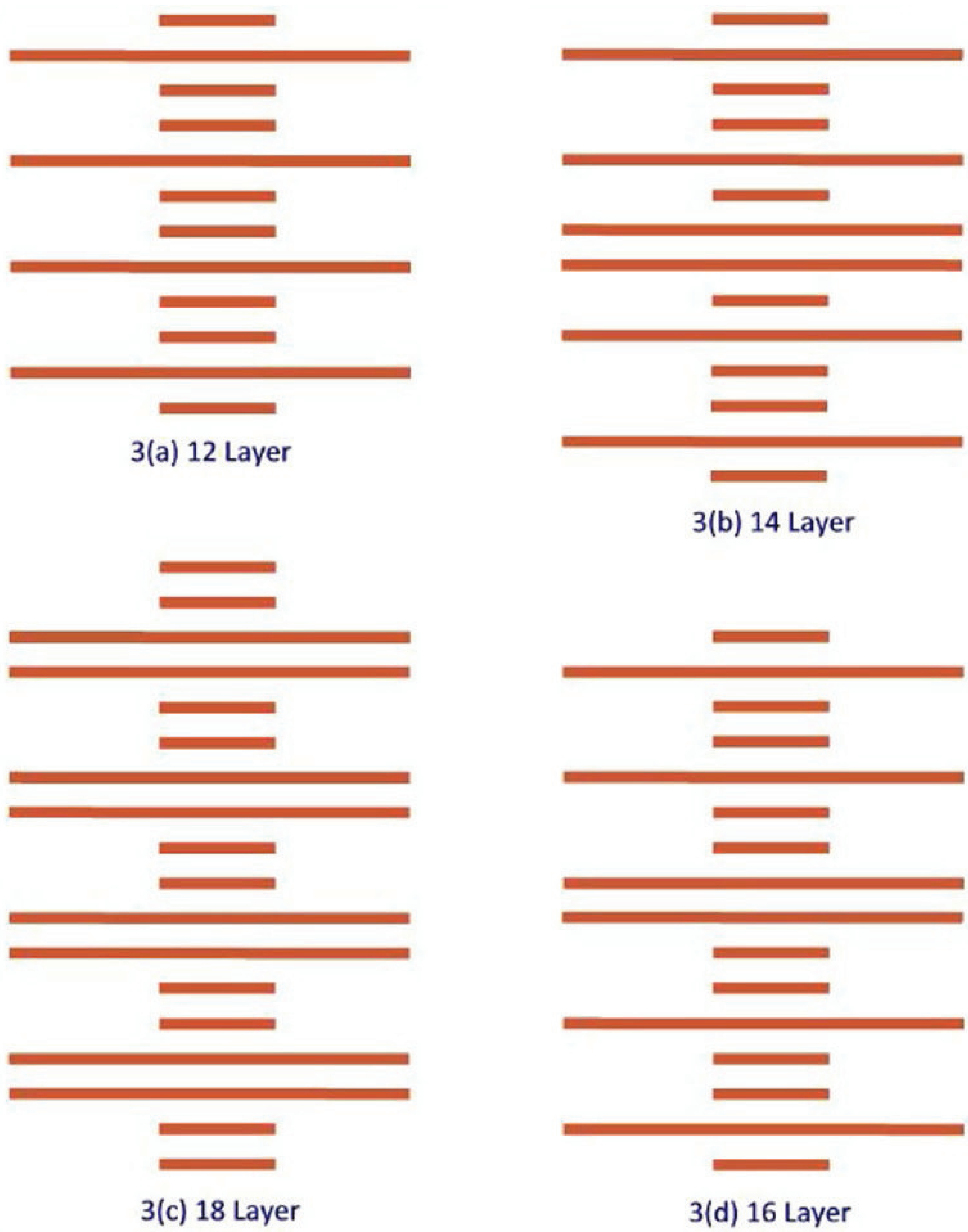


Figure 3: Image illustrating the signal/plane configuration for 12–18 layers.

layers pre-defined to get you started. Figure 3(c), is similar to Lee Ritchey's favorite stackup. This has all the good attributes that I have described, throughout this series, although 18 layers maybe overkill in some cases. But this basic configuration could be cut-down to 14 or 10 layers by removing groups of dual stripline layers.

Be creative. You can use more layers for planes, single or dual stripline routing layers but keep them symmetrical and most importantly, watch the return paths. The layer count always increments by even numbers. So, follow the basic rules I have set out in this stackup planning series and you cannot go wrong. Remember that the substrate is the most important component of the assembly, so let's get it right!

Points to Remember

- To minimize inductance, two conductors (signal traces or ground planes) that carry current in the same direction should be separated.
- Two conductors that carry current in the opposite direction (such as signal and ground planes or power and ground planes) should be positioned as close as possible.
- If power planes are used as reference planes, then the return current must transverse stitching capacitors in order to jump between ground and power planes.
- Use multiple ground planes, where possible, rather than power planes, in the stackup, to isolate signal layers.
- Place stitching ground vias close to every signal transition (via) to provide a short current return path.
- Spread numerous ground stitching vias around the board to connect the multiple ground planes.
- Don't use ground pours on signal layers as this reduces the impedance of nearby traces. If you must, in order to balance copper, separate the signal and pour by 20 mils.
- To determine the layer count, start with the route pitch. Technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable. Then calculate the stackup required for the desired characteristic and the differential impedances.
- A 10-layer board is similar to an eight layer with the addition of two more embedded signal layers. These are used to increase routability and to add planar capacitance.
- The methodology I have set out, in previous columns, can be used to construct higher layer count boards. **PCBDESIGN**

References

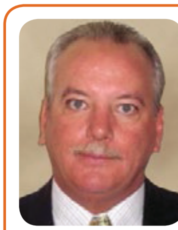
1. Barry Olney Beyond Design columns: Material Selection for SERDES Design, Material Selection for Digital Design, The Perfect Stackup for High-Speed Design, and Embedded Signal Routing.

2. Henry Ott, Electromagnetic Compatibility Engineering.

3. Lee Ritchey, Right First Time Design.

4. Howard Johnson, High-Speed Digital Design.

5. To download the ICD Stackup and PDN Planner, visit www.icd.com.au.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

Big Range of Behaviors for Tiny Graphene Pores

Researchers at MIT have created tiny pores in sheets of graphene that have an array of preferences and characteristics similar to those of ion channels in living cells.

Each graphene pore is less than 2 nanometers wide. Each is also uniquely selective, preferring to transport certain ions over others through the graphene layer.

To create pores in graphene, the group used chemical vapor deposition, a process typically used to produce thin films. In graphene, the process naturally creates tiny defects. Researchers may one day be able to tailor pores at the nanoscale to create ion-specific membranes for applications such as environmental sensing and trace metal mining.